Features

- Compatible with MCS®-51 Products
- 12K Bytes of In-System Programmable (ISP) Flash Program Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 10,000 Write/Erase Cycles
- 2K Bytes EEPROM Data Memory
  - Endurance: 100,000 Write/Erase Cycles
- 64-byte User Signature Array
- 2.7V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz (in x1 and x2 Modes)
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Enhanced UART Serial Port with Framing Error Detection and Automatic Address Recognition
- Enhanced SPI (Double Write/Read Buffered) Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Programmable Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Flexible ISP Programming (Byte and Page Modes)
  - Page Mode: 64 Bytes/Page for Code Memory, 32 Bytes/Page for Data Memory
- Four-level Enhanced Interrupt Controller
- Programmable and Fuseable x2 Clock Option
- Internal Power-on Reset
- 42-pin PDIP Package Option for Reduced EMC Emission
- Green (Pb/Halide-free) Packaging Option

8-bit Microcontroller with 12K Bytes Flash and 2K Bytes EEPROM

AT89S8253

1. Description

The AT89S8253 is a low-power, high-performance CMOS 8-bit microcontroller with 12K bytes of In-System Programmable (ISP) Flash program memory and 2K bytes of EEPROM data memory. The device is manufactured using Atmel's high-density non-volatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with downloadable Flash on a monolithic chip, the Atmel AT89S8253 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

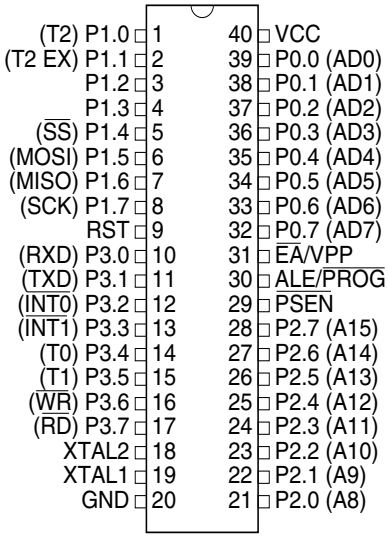
3286L–MICRO–8/08

The AT89S8253 provides the following standard features: 12K bytes of In-System Programmable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector, four-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8253 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

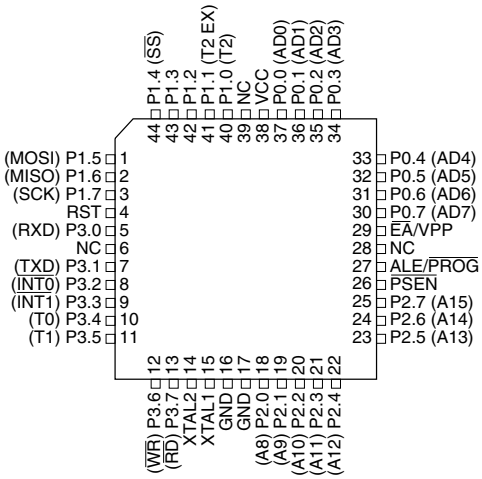
The on-board Flash/EEPROM is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from, unless one or more lock bits have been activated.

2. Pin Configurations

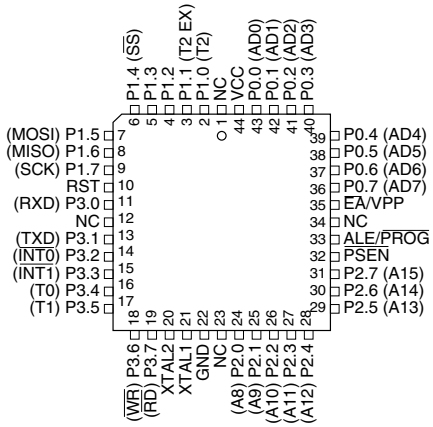
2.1 40P6 – 40-lead PDIP



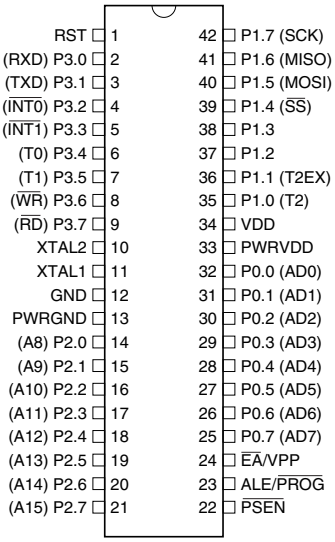
2.2 44A – 44-lead TQFP



2.3 44J – 44-lead PLCC



2.4 42PS6 – PDIP



3. Pin Description

3.1 VCC

Supply voltage (all packages except 42-PDIP).

3.2 GND

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program/data memories).

3.3 VDD

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program/data memories.

3.4 PWRVDD

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers.

The application board **must** connect both VDD and PWRVDD to the board supply voltage.

3.5 PWRGND

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal links. The application board **must** connect both GND and PWRGND to the board ground.

3.6 Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink six TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

3.7 Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source six TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the weak internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL},150 µA typical) because of the weak internal pull-ups.

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

3.8 Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source six TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the weak internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL},150 µA typical) because of the weak internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

3.9 Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source six TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the weak internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL},150 µA typical) because of the weak internal pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8253, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)[(1)]
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)[(1)]
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Note: 1. All pins in ports 1 and 2 and almost all pins in port 3 (the exceptions are P3.2 $\overline{\text{INT0}}$ and P3.3 $\overline{\text{INT1}}$) have their inputs disabled in the Power-down mode. Port pins P3.2 ($\overline{\text{INT0}}$) and P3.3 ($\overline{\text{INT1}}$) are active even in Power-down mode (to be able to sense an interrupt request to exit the Power-down mode) and as such still have their weak internal pull-ups turned on.

3.10 RST

Reset input. A high on this pin for at least two machine cycles while the oscillator is running resets the device.

3.11 ALE/$\overline{\text{PROG}}$

Address Latch Enable. ALE/$\overline{\text{PROG}}$ is an output pulse for latching the low byte of the address (on its falling edge) during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of the AUXR SFR at location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

3.12 $\overline{\text{PSEN}}$

Program Store Enable. $\overline{\text{PSEN}}$ is the read strobe to external program memory (active low).

When the AT89S8253 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

3.13 $\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

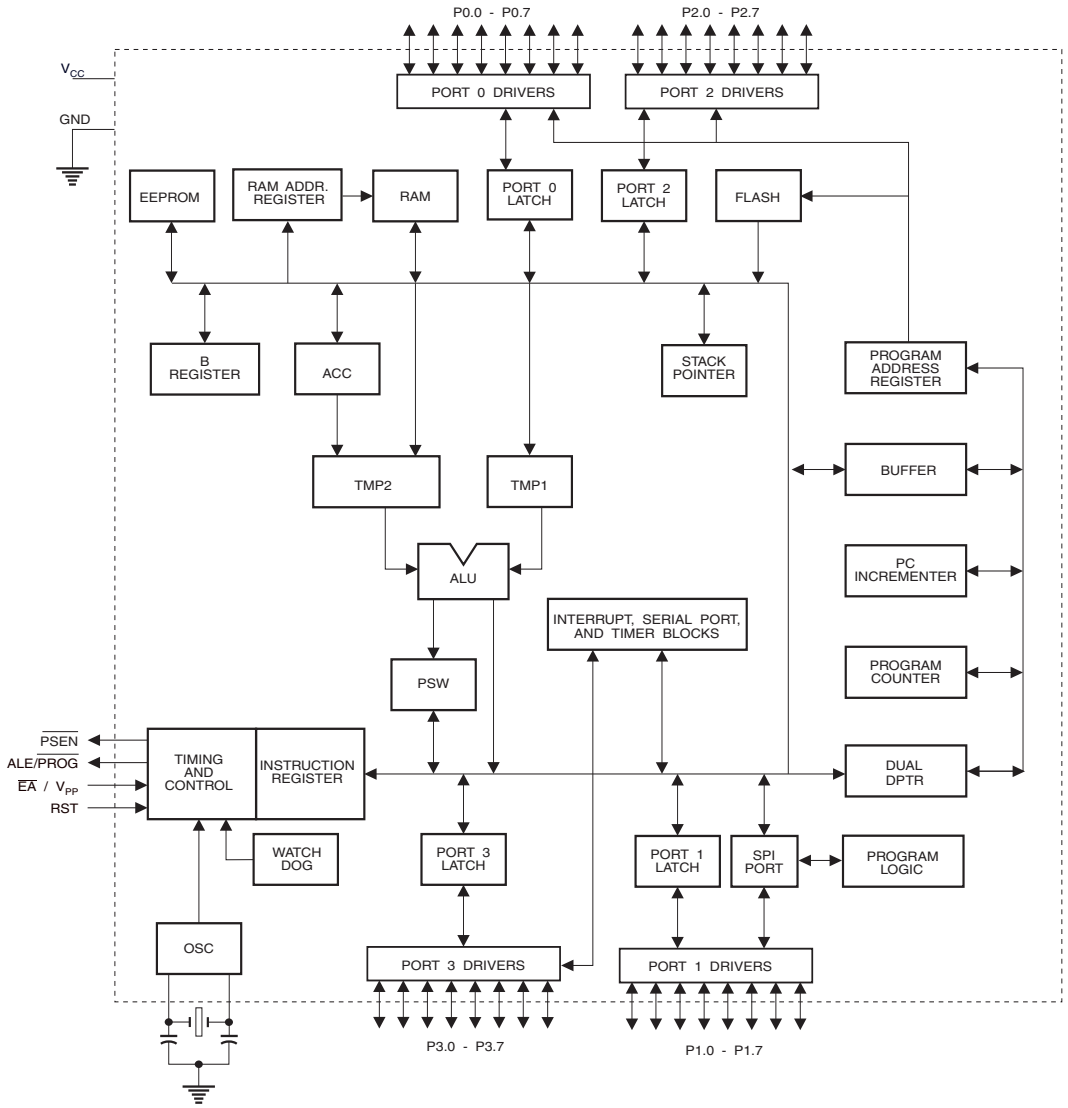
3.14 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

3.15 XTAL2

Output from the inverting oscillator amplifier.

4. Block Diagram



5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will generally return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Table 5-1. AT89S8253 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 00000100			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000	SADEN 00000000							0BFH
0B0H	P3 11111111							IPH XX000000	0B7H
0A8H	IE 0X000000	SADDR 00000000	SPSR 000XXX00						0AFH
0A0H	P2 11111111						WDTRST (Write Only)	WDTCON 0000 0000	0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						EECON XX000011		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXXXXXX0	CLKREG XXXXXXX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR ########	PCON 00XX0000	87H

Note: # means: 0 after cold reset and unchanged after warm reset.

5.1 Auxiliary Register

The AUXR Register contains a single active bit called DISALE.

Table 5-2. AUXR – Auxiliary Register

AUXR Address = 8EH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	Intel_Pwd_Exit	DISALE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
Intel_Pwd_Exit	When set, this bit configures the interrupt driven exit from power-down to resume execution on the rising edge of the interrupt signal. When this bit is cleared, the execution resumes after a self-timed interval (nominal 2 ms) referenced from the falling edge of the interrupt signal.
DISALE	When DISALE = 0, ALE is emitted at a constant rate of 1/6 the oscillator frequency (except during MOVX when 1 ALE pulse is missing). When DISALE = 1, ALE is active only during a MOVX or MOVC instruction.

5.2 Clock Register

The CLKREG register contains a single active bit called X2.

Table 5-3. CLKREG – Clock Register

CLKREG Address = 8FH — Reset Value = XXXX XXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	X2
Bit	7	6	5	4	3	2	1	0

Symbol	Function
X2	When X2 = 0, the oscillator frequency (at XTAL1 pin) is internally divided by 2 before it is used as the device system frequency. When X2 = 1, the divider by 2 is no longer used and the XTAL1 frequency becomes the device system frequency. This enables the user to choose a 6 MHz crystal instead of a 12 MHz crystal, for example, in order to reduce EMI.

5.3 SPI Registers

Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (see Table 14-1 on page 25) and SPSR (see Table 14-2 on page 26). The SPI data bits are contained in the SPDR register. In normal SPI mode, writing the SPI data register during serial data transfer sets the Write Collision bit (WCOL) in the SPSR register. In enhanced SPI mode, the SPDR is also write double-buffered because WCOL works as a Write Buffer Full Flag instead of being a collision flag. The values in SPDR are not changed by Reset.

5.4 Interrupt Registers

The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Four priorities can be set for each of the six interrupt sources in the IP and IPH registers.

IPH bits have the same functions as IP bits, except IPH has higher priority than IP. By using IPH in conjunction with IP, a priority level of 0, 1, 2, or 3 may be set for each interrupt.

5.5 Dual Data Pointer Registers

To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H - 83H and DP1 at 84H - 85H. Bit DPS = 0 in SFR EECON selects DP0 and DPS = 1 selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

5.6 Power Off Flag

The Power Off Flag (POF), located at bit_4 (PCON.4) in the PCON SFR. POF, is set to “1” during power up. It can be set and reset under software control and is not affected by RESET.

6. Data Memory – EEPROM and RAM

The AT89S8253 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the EECON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to “0”.

During program execution mode (using the MOVX instruction) there is an auto-erase capability at the byte level. This means that the user can update or modify a single EEPROM byte location in real-time without affecting any other bytes.

The EEMWE bit in the EECON register needs to be set to “1” before any byte location in the EEPROM can be written. User software should reset EEMWE bit to “0” if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 4 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{\text{BSY}}$ bit (read-only) in SFR EECON. RDY/$\overline{\text{BSY}}$ = 0 means programming is still in progress and RDY/$\overline{\text{BSY}}$ = 1 means an EEPROM write cycle is completed and another write cycle can be initiated. Bit EELD in EECON controls whether the next MOVX instruction will only load the write buffer of the EEPROM or will actually start the programming cycle. By setting EELD, only load will occur. Before the last MOVX in a given page of 32 bytes, EELD should be cleared so that after the last MOVX the entire page will be programmed at the same time. This way, 32 bytes will only require 4 ms of programming time instead of 128 ms required in single byte programming.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

6.1 Memory Control Register

The EECON register contains control bits for the 2K bytes of on-chip data EEPROM. It also contains the control bit for the dual data pointer.

Table 6-1. EECON – Data EEPROM Control Register

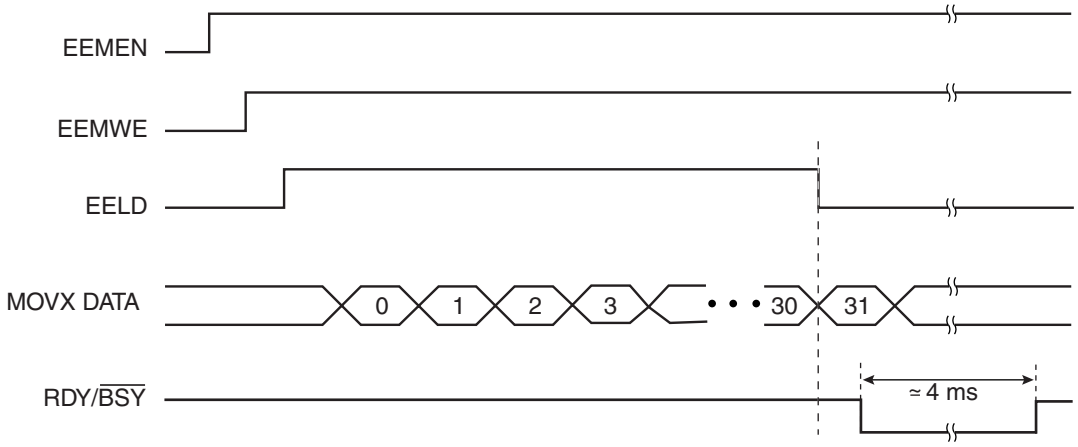
EECON Address = 96H — Reset Value = XX00 0011B

Not Bit Addressable

Bit	–	–	EELD	EEMWE	EEMEN	DPS	RDY/$\overline{BSY}$	$\overline{WRTINH}$
	7	6	5	4	3	2	1	0

Symbol	Function
EELD	EEPROM data memory load enable bit. Used to implement Page Mode Write. A MOVX instruction writing into the data EEPROM will not initiate the programming cycle if this bit is set, rather it will just load data into the volatile data buffer of the data EEPROM memory. Before the last MOVX, reset this bit and the data EEPROM will program all the bytes previously loaded on the same page of the address given by the last MOVX instruction.
EEMWE	EEPROM data memory write enable bit. Set this bit to 1 before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to 0 after EEPROM write is completed.
EEMEN	Internal EEPROM access enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory if the address used is less than 2K. When EEMEN = 0 or the address used is □ 2K, MOVX with DPTR accesses external data memory.
DPS	Data pointer register select. DPS = 0 selects the first bank of data pointer register, DP0, and DPS = 1 selects the second bank, DP1.
RDY/$\overline{BSY}$	RDY/$\overline{BSY}$ (Ready/$\overline{Busy}$) flag for the data EEPROM memory. This is a read-only bit which is cleared by hardware during the programming cycle of the on-chip EEPROM. It is also set by hardware when the programming is completed. Note that RDY/$\overline{BSY}$ will be cleared long after the completion of the MOVX instruction which has initiated the programming cycle.
$\overline{WRTINH}$	$\overline{WRTINH}$ (Write Inhibit) is a READ-ONLY bit which is cleared by hardware when V_{cc} is too low for the programming cycle of the on-chip EEPROM to be executed. When this bit is cleared, an ongoing programming cycle will be aborted or a new programming cycle will not start.

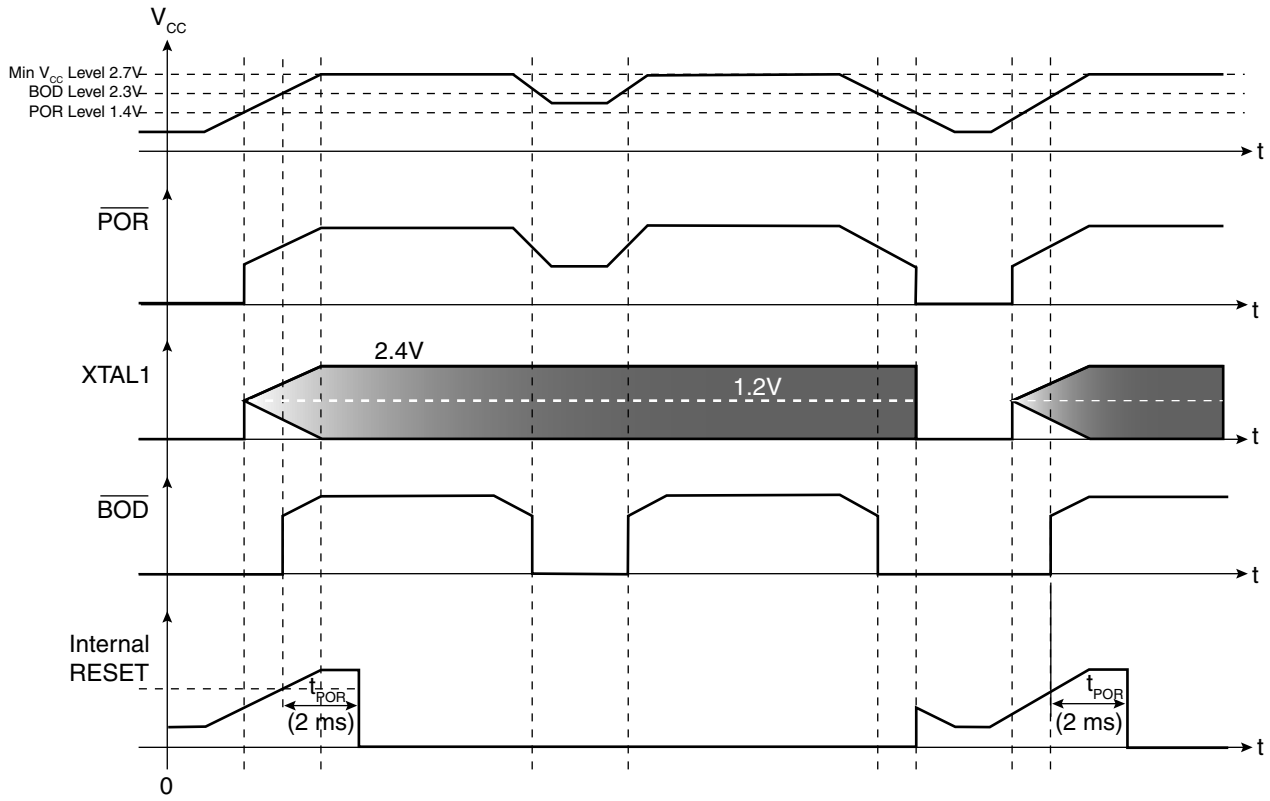
Figure 6-1. Data EEPROM Write Sequence



7. Power-On Reset

A Power-On Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. When V_{CC} reaches the Power-on Reset threshold voltage, the POR delay counter determines how long the device is kept in POR after V_{CC} rise, nominally 2 ms. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-On Reset (i.e. a cold reset) will set the POF flag in PCON.

Figure 7-1. Power-up and Brown-out Detection Sequence



7.1 Brown-out Reset

The AT89S8253 has an on-chip Brown-out Detection (BOD) circuit for monitoring the V_{CC} level during operation by comparing it to a fixed trigger level of 2.4V (max). The trigger level for the BOD is nominally 2.2V. The purpose of the BOD is to ensure that if V_{CC} fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution. When V_{CC} decreases to a value below the trigger level, the Brown-out Reset is immediately activated. When V_{CC} increases above the trigger level, the BOD delay counter starts the MCU after the timeout period has expired in approximately 2 ms.

8. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) counts instruction cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K instruction cycles. The available timer periods are shown in Table 8-1. The WDT time-out period is dependent upon the external clock frequency.

The WDT is disabled by Power-on Reset and during Power-down mode. When WDT times out without being serviced or disabled, an internal RST pulse is generated to reset the CPU. See Table 8-1 for the WDT period selections.

Table 8-1. Watchdog Timer Time-out Period Selection

WDT Prescaler Bits			Period (Nominal for F_{CLK} = 12 MHz)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

8.1 Watchdog Control Register

The WDTCON register contains control bits for the Watchdog Timer (shown in Table 8-2).

Table 8-2. WDTCON – Watchdog Control Register

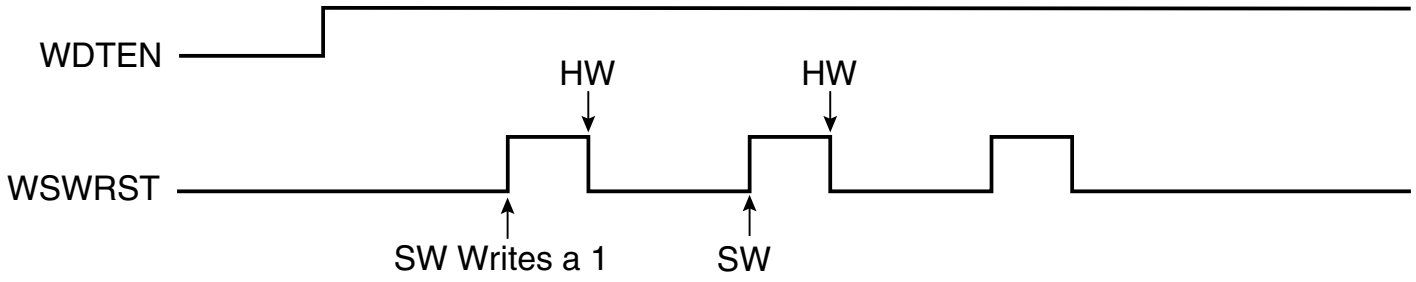
WDTCON Address = A7H — Reset Value = 0000 0000B

Not Bit Addressable

	PS2	PS1	PS0	WDIDLE	DISRTO	HWDT	WSWRST	WDTEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler bits for the watchdog timer (WDT). When all three bits are cleared to 0, the watchdog timer has a nominal period of 16K machine cycles, (i.e. 16 ms at a XTAL frequency of 12 MHz in normal mode or 6 MHz in x2 mode). When all three bits are set to 1, the nominal period is 2048K machine cycles, (i.e. 2048 ms at 12 MHz clock frequency in normal mode or 6 MHz in x2 mode).
WDIDLE	Enable/disable the Watchdog Timer in IDLE mode. When WDIDLE = 0, WDT continues to count in IDLE mode. When WDIDLE = 1, WDT freezes while the device is in IDLE mode.
DISRTO	Enable/disable the WDT-driven Reset Out (WDT drives the RST pin). When DISRTO = 0, the RST pin is driven high after WDT times out and the entire board is reset. When DISRTO = 1, the RST pin remains only as an input and the WDT resets only the microcontroller internally after WDT times out.
HWDT	Hardware mode select for the WDT. When HWDT = 0, the WDT can be turned on/off by simply setting or clearing WDTEN in the same register (this is the software mode for WDT). When HWDT = 1, the WDT has to be set by writing the sequence 1EH/E1H to the WDTRST register (with address 0A6H) and after being set in this way, WDT cannot be turned off except by reset, warm or cold (this is the hardware mode for WDT). To prevent the hardware WDT from resetting the entire device, the same sequence 1EH/E1H must be written to the same WDTRST SFR before the timeout interval.
WSWRST	Watchdog software reset bit. If HWDT = 0 (i.e. WDT is in software controlled mode), when set by software, this bit resets WDT. After being set by software, WSWRST is reset by hardware during the next machine cycle. If HWDT = 1, this bit has no effect, and if set by software, it will not be cleared by hardware.
WDTEN	Watchdog software enable bit. When HWDT = 0 (i.e. WDT is in software-controlled mode), this bit enables WDT when set to 1 and disables WDT when cleared to 0 (it does not reset WDT in this case, but just freezes the existing counter state). If HWDT = 1, this bit is READ-ONLY and reflects the status of the WDT (whether it is running or not).

Figure 8-1. Software Mode – Watchdog Timer Sequence



9. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8253 operate the same way as Timer 0 and Timer 1 in the AT89S51 and AT89S52. For more detailed information on the Timer/Counter operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

10. Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (see Table 10-2 on page 15). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 10-2.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Table 10-1. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Table 10-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

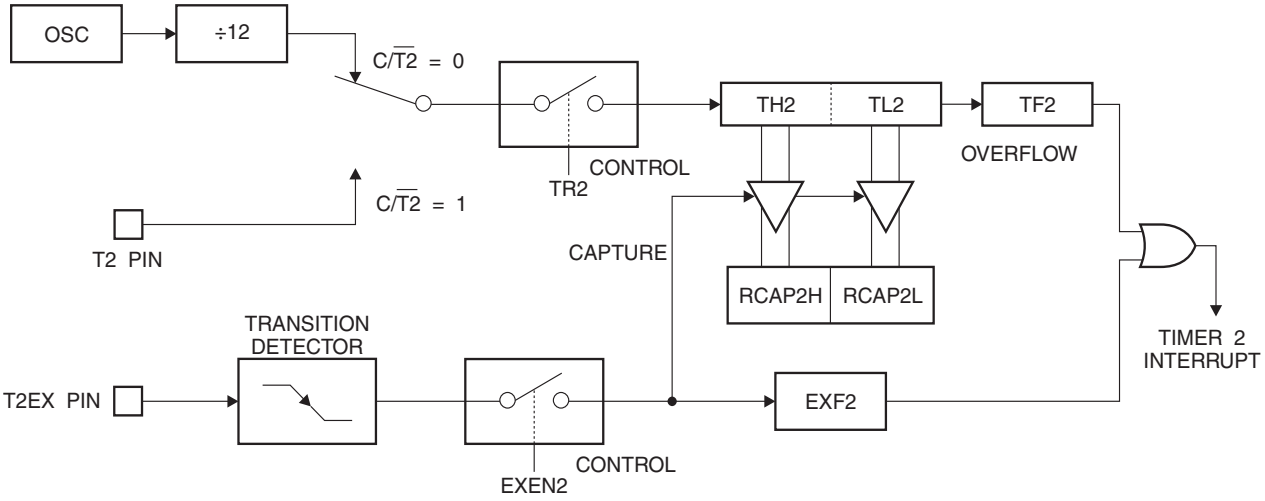
10.1 Timer 2 Registers

Control and status bits are contained in registers T2CON (see Table 10-2) and T2MOD (see Table 10-3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

10.2 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 10-1.

Figure 10-1. Timer 2 in Capture Mode



10.3 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 10-3). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Table 10-3. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 10-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 10-3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 10-2. Timer 2 in Auto Reload Mode (DCEN = 0)

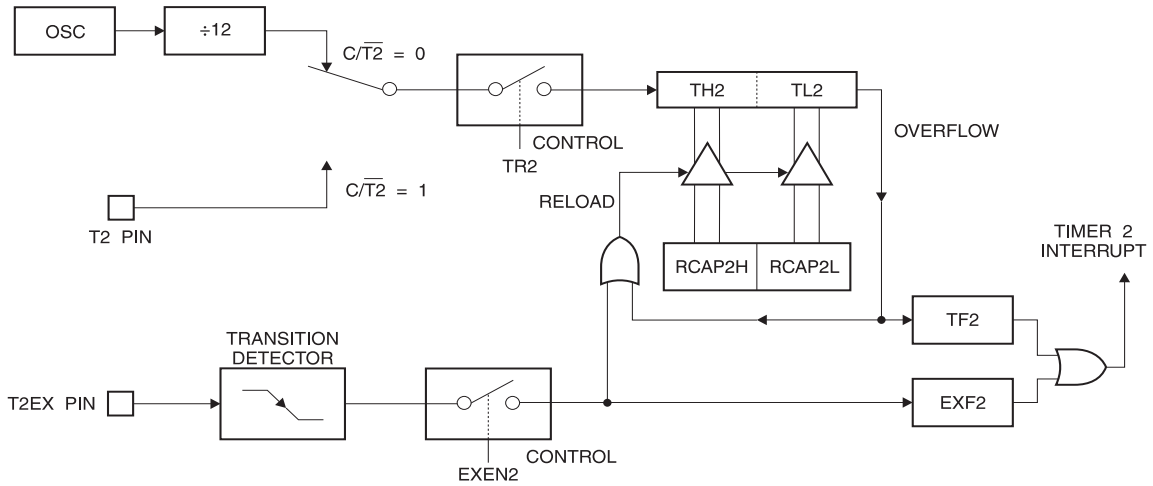


Figure 10-3. Timer 2 Auto Reload Mode (DCEN = 1 Timer 2 Auto Reload Mode (DCEN = 1)

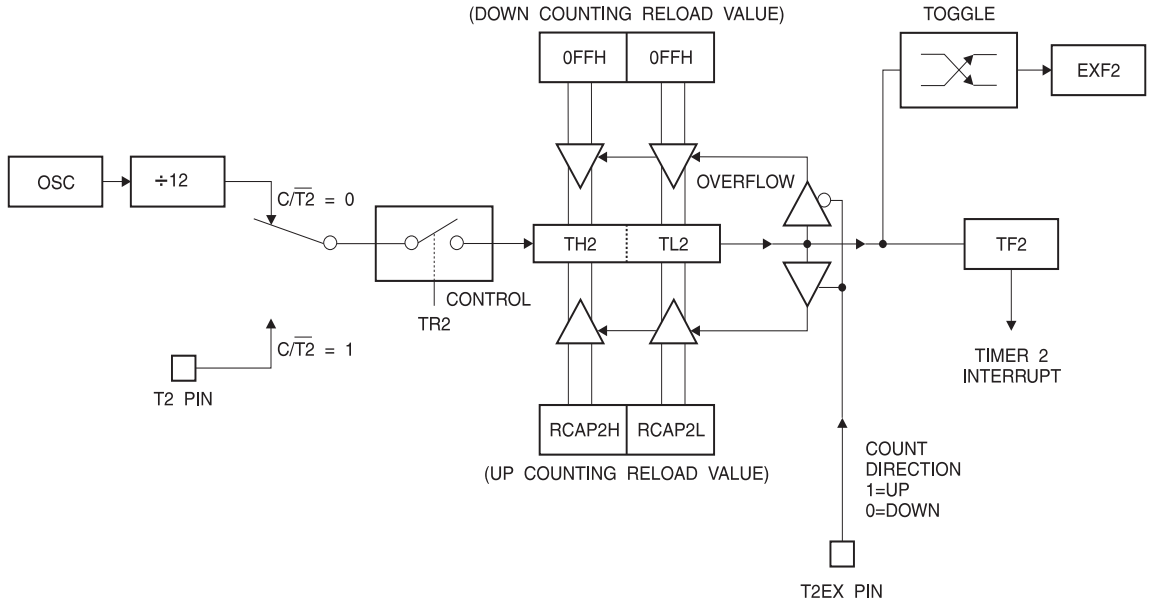
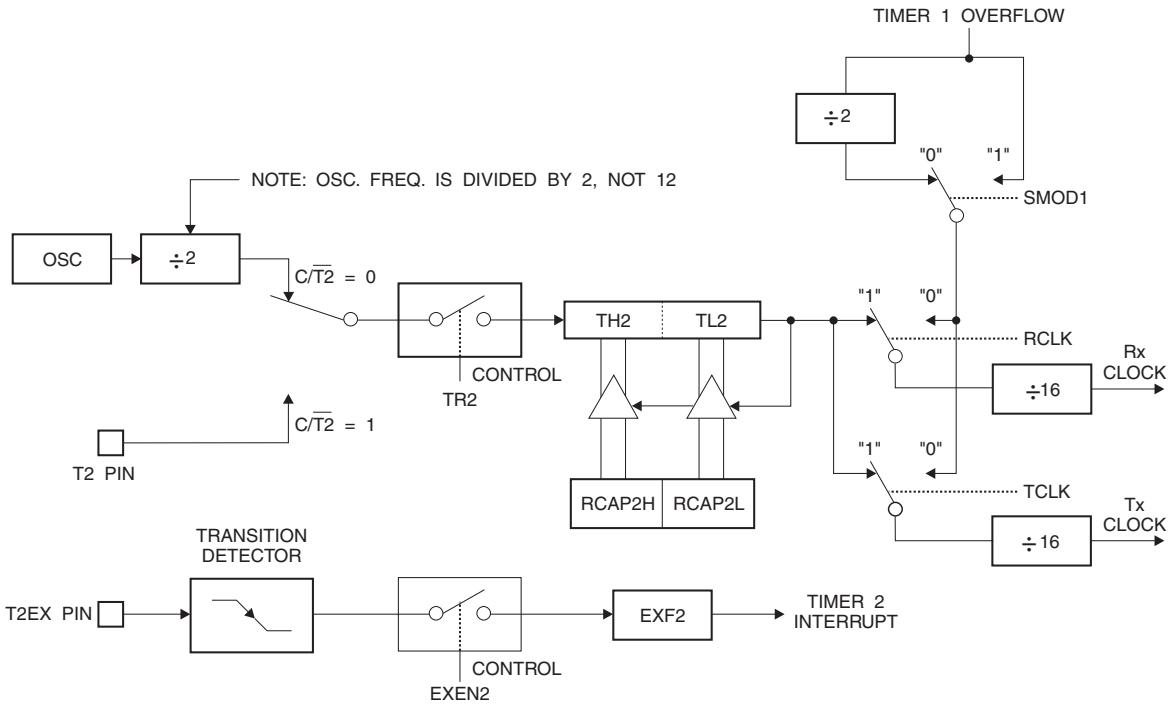


Figure 10-4. Timer 2 in Baud Rate Generator Mode



11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 10-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 10-4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation (CP/$\overline{T2}$ = 0). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 10-4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

12. Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 12-1. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16 MHz operating frequency).

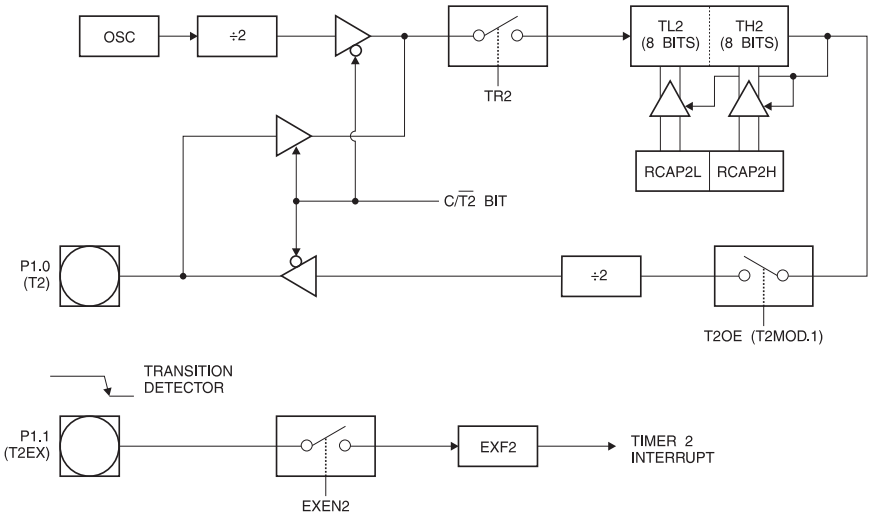
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 12-1. Timer 2 in Clock-out Mode



13. UART

The UART in the AT89S8253 operates the same way as the UART in the AT89S51 and AT89S52. For more detailed information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

13.1 Enhanced UART

In addition to all of its usual modes, the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software.

13.1.1 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9-bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data.

The 8-bit mode is called mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1101

Given = 1100 00X0

Slave 1 SADDR = 1100 0000

SADEN = 1111 1110

Given = 1100 000X

In the previous example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1001
	Given	= 1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	1111 1010
	Given	= 1110 0X0X
Slave 2	SADDR =	1110 0000
	SADEN =	1111 1100
	Given	= 1110 00XX

In the previous example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

Table 13-1. PCON – Power Control Register

PCON Address = 87H — Reset Value = 00xx 0000B

Bit Addressable

	SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in Modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 1, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
POF	Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power-down bit. Setting this bit activates power-down operation.
IDL	Idle Mode bit. Setting this bit activates Idle mode operation

Table 13-2. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	T1	RI
Bit	7	6	5	4	3	2	1	0
	(SMOD0 = 0/1)[1]							

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD0.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 SM0 — SM1 — Mode — Description — Baud Rate[2] 0 — 0 — 0 — shift register — $f_{osc}/12$ 0 — 1 — 1 — 8-bit UART — variable 1 — 0 — 2 — 9-bit UART — $f_{osc}/64$ or $f_{osc}/32$ 1 — 1 — 3 — 9-bit UART — variable
SM2	Enables the Automatic Address Recognition feature in modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD0 is located at PCON.6.

2. f_{osc} = oscillator frequency.

14. Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8253 and peripheral devices or between multiple AT89S8253 devices. The AT89S8253 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- Maximum Bit Frequency = f/4 (f/2 if in x2 Clock Mode)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates in Master Mode
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Double-Buffered Receive
- Double-Buffered Transmit (Enhanced Mode only)
- Wakeup from Idle Mode (Slave Mode only)

The interconnection between master and slave CPUs with SPI is shown in Figure 14-1. The four pins in the interface are Master-In/Slave-Out (MISO), Master-Out/Slave-In (MOSI), Shift Clock (SCK), and Slave Select ($\overline{SS}$). The SCK pin is the clock output in master mode, but is the clock input in slave mode. The MSTR bit in SPCR determines the directions of MISO and MOSI. Also notice that MOSI connects to MOSI and MISO to MISO. In master mode, $\overline{SS}$/P1.4 is ignored and may be used as a general-purpose input or output. In slave mode, $\overline{SS}$ must be driven low to select an individual device as a slave. When $\overline{SS}$ is driven high, the slave's SPI port is deactivated and the MOSI/P1.5 pin can be used as a general-purpose input.

Figure 14-1. SPI Master-Slave Interconnection

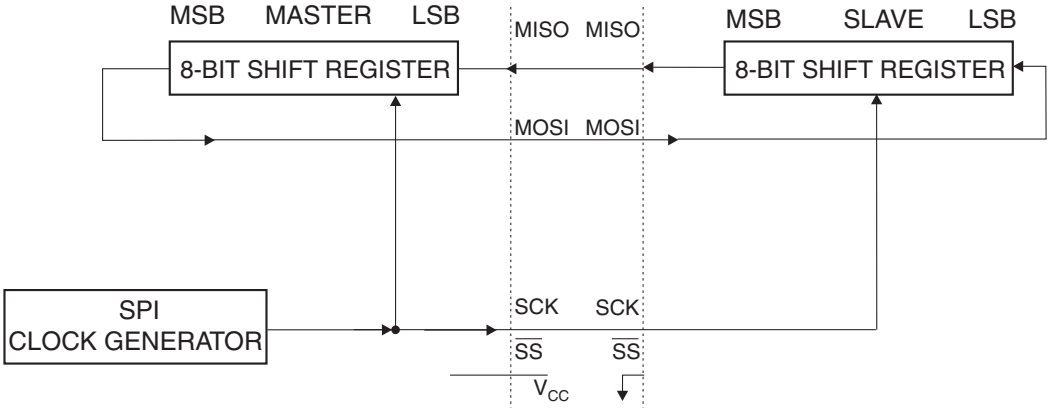
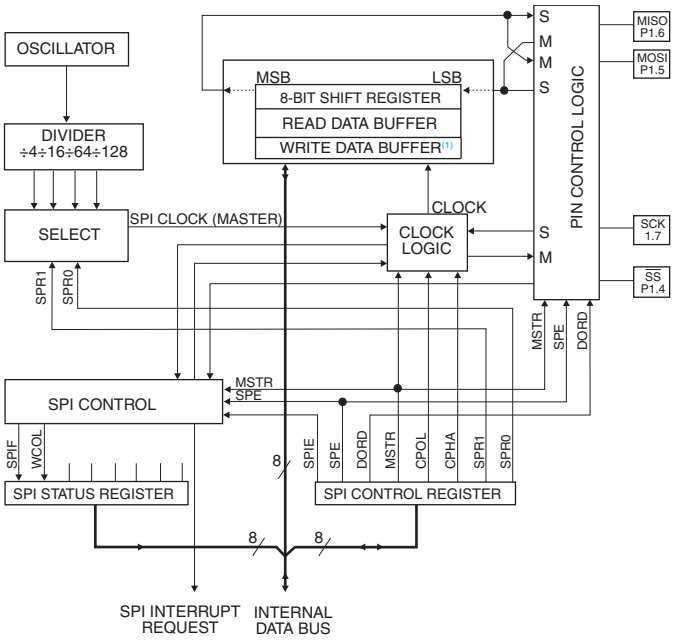


Figure 14-2. SPI Block Diagram



Note: 1. The Write Data Buffer is only used in enhanced SPI mode.

The SPI has two modes of operation: normal (non-buffered write) and enhanced (buffered write). In normal mode, writing to the SPI data register (SPDR) of the master CPU starts the SPI clock generator and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. Transmission may start after an initial delay while the clock generator waits for the next full bit slot of the specified baud rate. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF) and transferring the received byte to the read buffer (SPDR). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested. Note that SPDR refers to either the write data buffer or the read data buffer, depending on whether the access is a write or read. In normal mode, because the write buffer is transparent (and a write access to SPDR will be directed to the shift buffer), any attempt to write to SPDR while a transmission is in progress will result in a write collision with WCOL set. However, the transmission will still complete normally, but the new byte will be ignored and a new write access to SPDR will be necessary.

Enhanced mode is similar to normal mode except that the write buffer holds the next byte to be transmitted. Writing to SPDR loads the write buffer and sets WCOL to signify that the buffer is full and any further writes will overwrite the buffer. WCOL is cleared by hardware when the buffered byte is loaded into the shift register and transmission begins. If the master SPI is currently idle, i.e. if this is the first byte, then after loading SPDR, transmission of the byte starts and WCOL is cleared immediately. While this byte is transmitting, the next byte may be written to SPDR. The Load Enable flag (LDEN) in SPSR can be used to determine when transmission has started. LDEN is asserted during the first four bit slots of a SPI transfer. The master CPU should first check that LDEN is set and that WCOL is cleared before loading the next byte. In enhanced mode, if WCOL is set when a transfer completes, i.e. the next byte is available, then the SPI immediately loads the buffered byte into the shift register, resets WCOL, and continues transmission without stopping and restarting the clock generator. As long as the CPU can keep the write buffer full in this manner, multiple bytes may be transferred with minimal latency between bytes.

Table 14-1. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 0100B

Not Bit Addressable

	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI interrupt enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/slave select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects slave SPI mode.
CPOL	Clock polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI clock phase and polarity control.
CPHA	Clock phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI clock phase and polarity control.
SPR0 SPR1	SPI clock rate select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{OSC.}$, is as follows: **SPR1SPR0SCK** 00f/4 (f/2 in x2 mode) 01f/16 (f/8 in x2 mode) 10f/64 (f/32 in x2 mode) 11f/128 (f/64 in x2 mode)

Notes:
1. Set up the clock mode before enabling the SPI: set all bits needed in SPCR except the SPE bit, then set SPE.
2. Enable the master SPI prior to the slave device.
3. Slave echoes master on next Tx if not loaded with new data.

Table 14-2. SPSR – SPI Status Register

SPSR Address = AAH

Reset Value = 000X XX00B

Not Bit Addressable

	SPIF	WCOL	LDEN	–	–	–	DISSO	ENH
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SPI interrupt flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register **followed by** reading/writing the SPI data register.
WCOL	When ENH = 0: Write collision flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register **followed by** reading/writing the SPI data register. When ENH = 1: WCOL works in Enhanced mode as Tx Buffer Full. Writing during WCOL = 1 in enhanced mode will overwrite the waiting data already present in the Tx Buffer. In this mode, WCOL is no longer reset by the SPIF reset but is reset when the write buffer has been unloaded into the serial shift register.
LDEN	Load enable for the Tx buffer in enhanced SPI mode. When ENH is set, it is safe to load the Tx Buffer while LDEN = 1 and WCOL = 0. LDEN is high during bits 0 - 3 and is low during bits 4 - 7 of the SPI serial byte transmission time frame.
DISSO	Disable slave output bit. When set, this bit causes the MISO pin to be tri-stated so more than one slave device can share the same interface with a single master. Normally, the first byte in a transmission could be the slave address and only the selected slave should clear its DISSO bit.
ENH	Enhanced SPI mode select bit. When ENH = 0, SPI is in normal mode, i.e. without write double buffering. When ENH = 1, SPI is in enhanced mode with write double buffering. The Tx buffer shares the same address with the SPDR register.

Table 14-3. SPDR – SPI Data Register

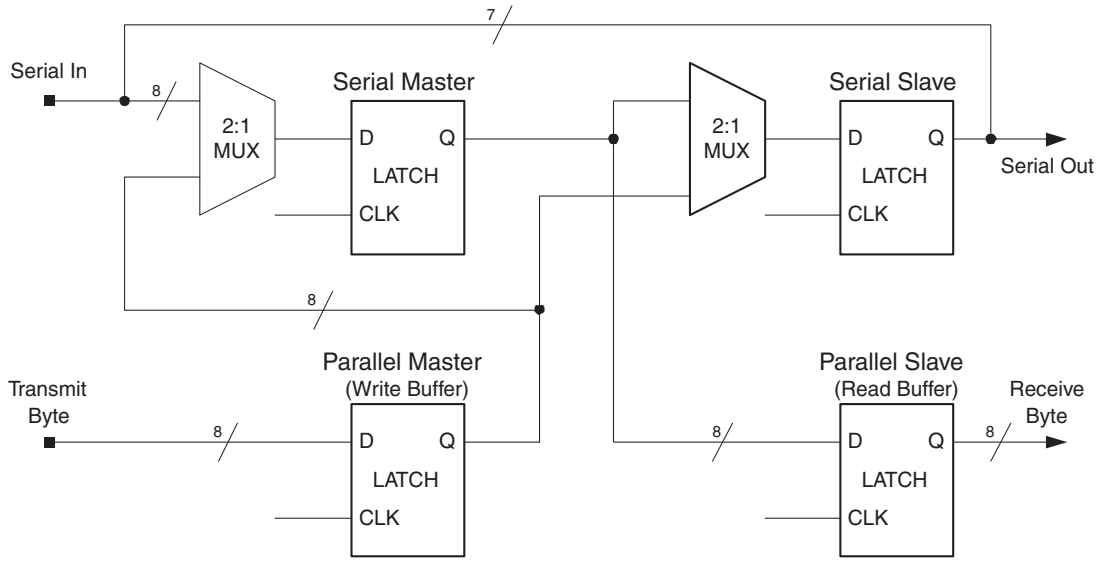
SPDR Address = 86H

Not Bit Addressable

Reset Value = 00H (after cold reset)
unchanged (after warm reset)

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

Figure 14-3. SPI Shift Register Diagram



The CPHA (Clock PHAse), CPOL (Clock POLarity), and SPR (Serial Peripheral clock Rate = baud rate) bits in SPCR control the shape and rate of SCK. The two SPR bits provide four possible clock rates when the SPI is in master mode. In slave mode, the SPI will operate at the rate of the incoming SCK as long as it does not exceed the maximum bit rate. There are also four possible combinations of SCK phase and polarity with respect to the serial data. CPHA and CPOL determine which format is used for transmission. The SPI data transfer formats are shown in Figure 14-4 and Figure 14-5. To prevent glitches on SCK from disrupting the interface, CPHA, CPOL, and SPR should be set up before the interface is enabled, and the master device should be enabled before the slave device(s).

Table 14-4. SPI **Master** Characteristics

Symbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Period	41.6		ns
t_{SCK}	Serial Clock Cycle Time	$4t_{CLCL}$		ns
t_{SHSL}	Clock High Time	$t_{SCK}/2 - 25$		ns
t_{SLSH}	Clock Low Time	$t_{SCK}/2 - 25$		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns
t_{SIS}	Serial Input Setup Time	10		ns
t_{SIH}	Serial Input Hold Time	10		ns
t_{SOH}	Serial Output Hold Time		10	ns
t_{SOV}	Serial Output Valid Time		35	ns

Table 14-5. SPI **Slave** Characteristics

Symbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Period	41.6		ns
t_{SCK}	Serial Clock Cycle Time	$4t_{CLCL}$		ns
t_{SHSL}	Clock High Time	1.5 t_{CLCL} - 25		ns
t_{SLSH}	Clock Low Time	1.5 t_{CLCL} - 25		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns
t_{SIS}	Serial Input Setup Time	10		ns
t_{SIH}	Serial Input Hold Time	10		ns
t_{SOH}	Serial Output Hold Time		10	ns
t_{SOV}	Serial Output Valid Time		35	ns
t_{SOE}	Output Enable Time		10	ns
t_{SOX}	Output Disable Time		25	ns
t_{SSE}	Slave Enable Lead Time	4 t_{CLCL} +50		ns
t_{SSD}	Slave Disable Lag Time	0		ns

Figure 14-4. SPI Master Timing (CPHA = 0)

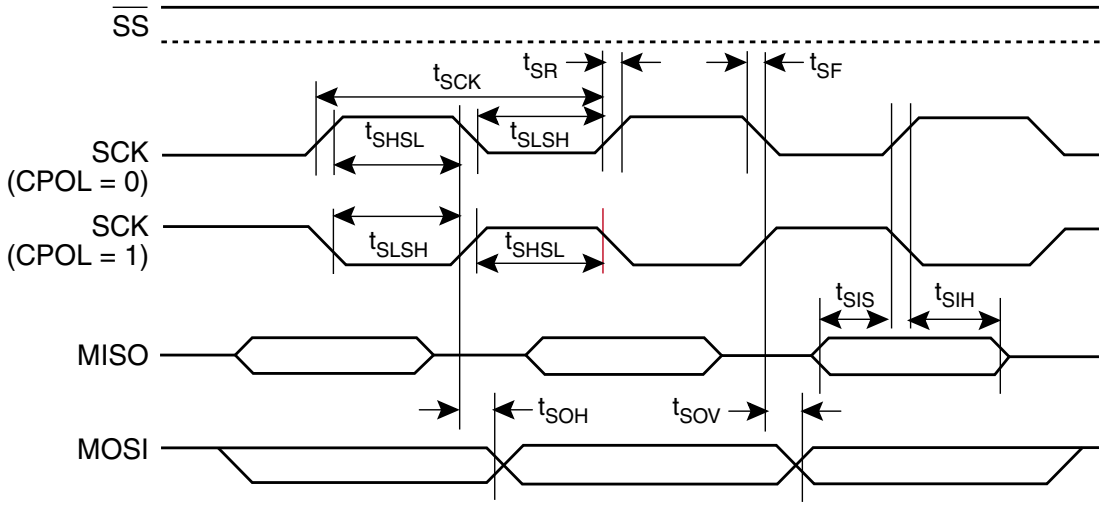


Figure 14-5. SPI Slave Timing (CPHA = 0)

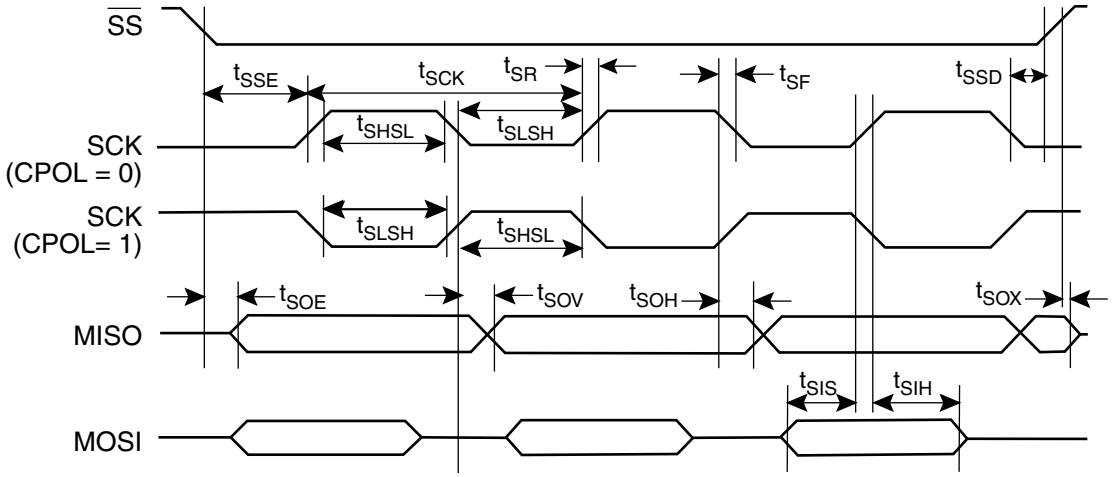


Figure 14-6. SPI Master Timing (CPHA = 1)

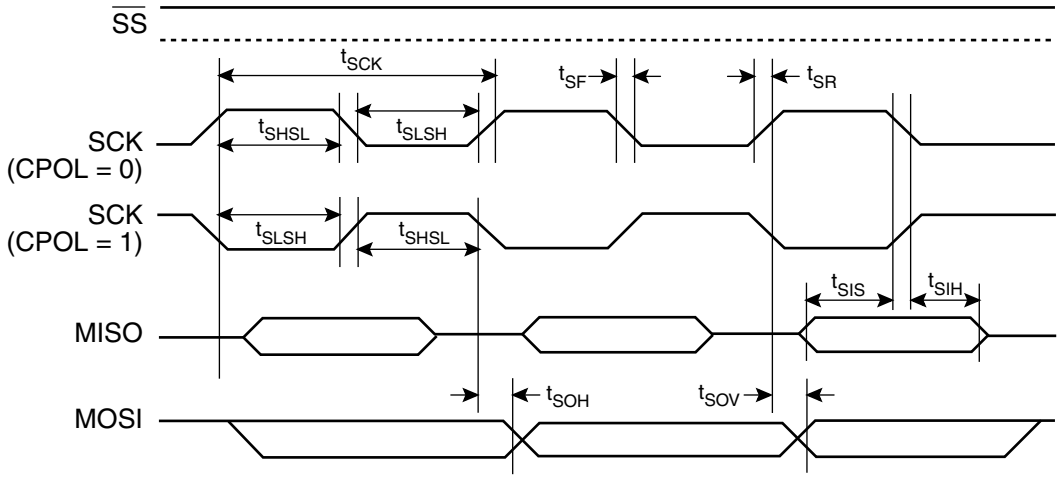


Figure 14-7. SPI Slave Timing (CPHA = 1)

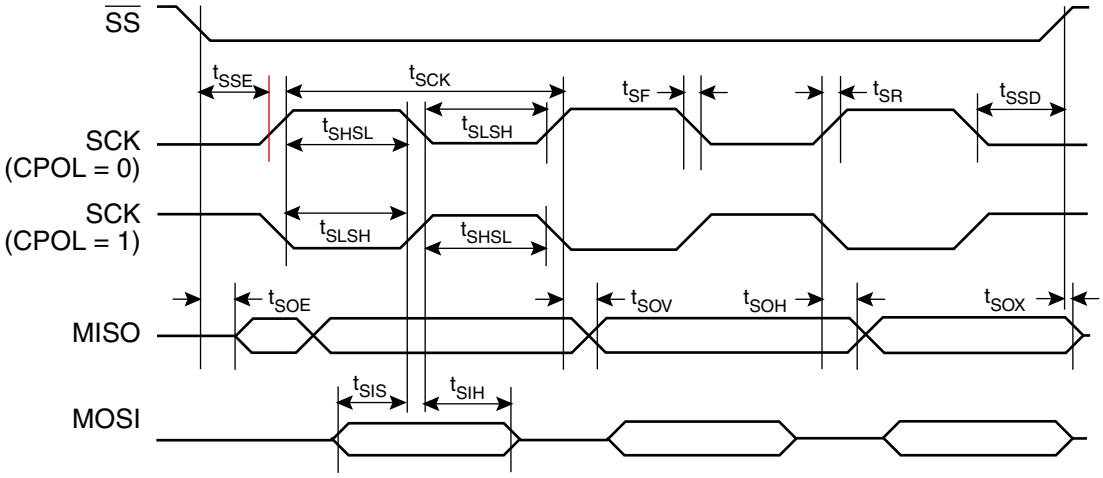
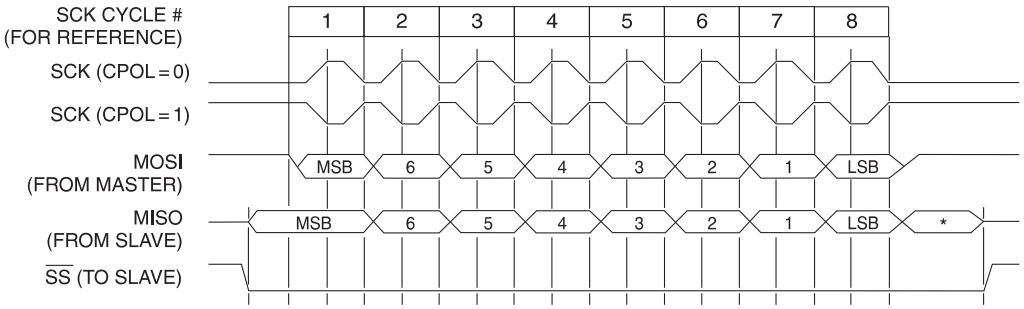
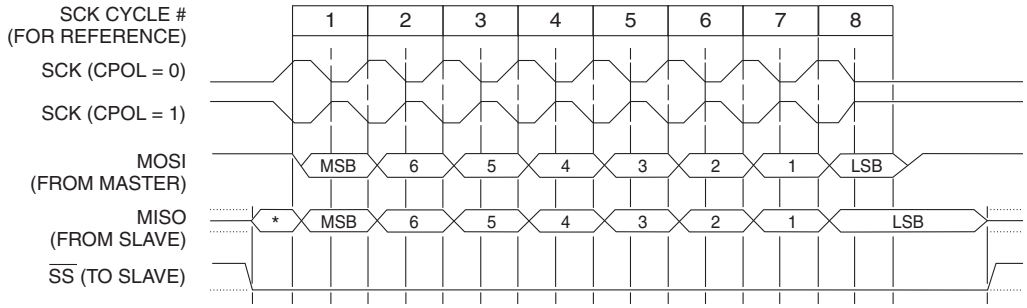


Figure 14-8. SPI Transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received

Figure 14-9. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character

15. Interrupts

The AT89S8253 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 15-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 15-1 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The serial interrupt is the logical OR of bits RI and TI in register SCON and also bit SPIF in SPSR (if SPIE in SPCR is set). None of these flags is cleared by hardware when the service routine is vectored to. The service routine may have to determine whether the UART or SPI generated the interrupt.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Interrupt	Source	Vector Address
System Reset	RST or POR or BOD	0000H
External Interrupt 0	IE0	0003H
Timer 0 Overflow	TF0	000BH
External Interrupt 1	IE1	0013H
Timer 1 Overflow	TF1	001BH
Serial Port	RI or TI or SPIF	0023H

Table 15-1. Interrupt Enable (IE) Register

IE Address = A8H — Reset Value = 0X00 0000B

Bit Addressable

EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

Table 15-2. IP – Interrupt Priority Register

IP = B8H — Reset Value = XX00 0000B

Bit Addressable

	–	–	PT2	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PT2	Timer 2 Interrupt Priority Low
PS	Serial Port Interrupt Priority Low
PT1	Timer 1 Interrupt Priority Low
PX1	External Interrupt 1 Priority Low
PT0	Timer 0 Interrupt Priority Low
PX0	External Interrupt 0 Priority Low

Table 15-3. IPH – Interrupt Priority High Register

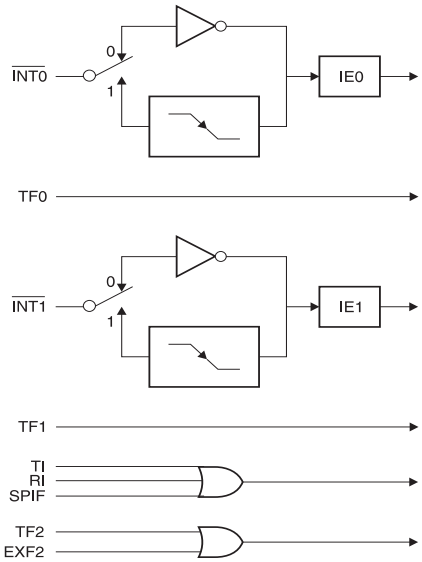
IPH = B7H — Reset Value = XX00 0000B

Not Bit Addressable

	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PT2H	Timer 2 Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

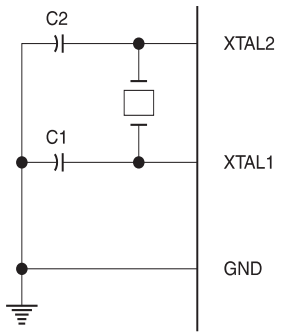
Figure 15-1. Interrupt Sources



16. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 16-1. Either a quartz crystal or ceramic resonator may be used. Figures 16-2 and 16-3 illustrate the relationship between sample clock loading and the respective resulting clock amplitudes.

Figure 16-1. Oscillator Connections



Note: C1, C2 = 5 pF ± 5 pF for Crystals
= 5 pF ± 5 pF for Ceramic Resonators

Figure 16-2. Quartz Crystal Clock Source

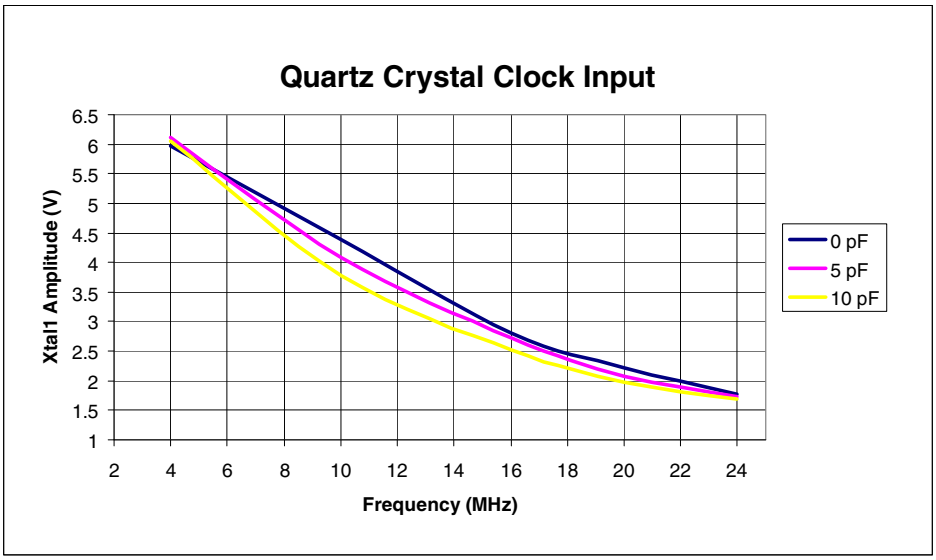
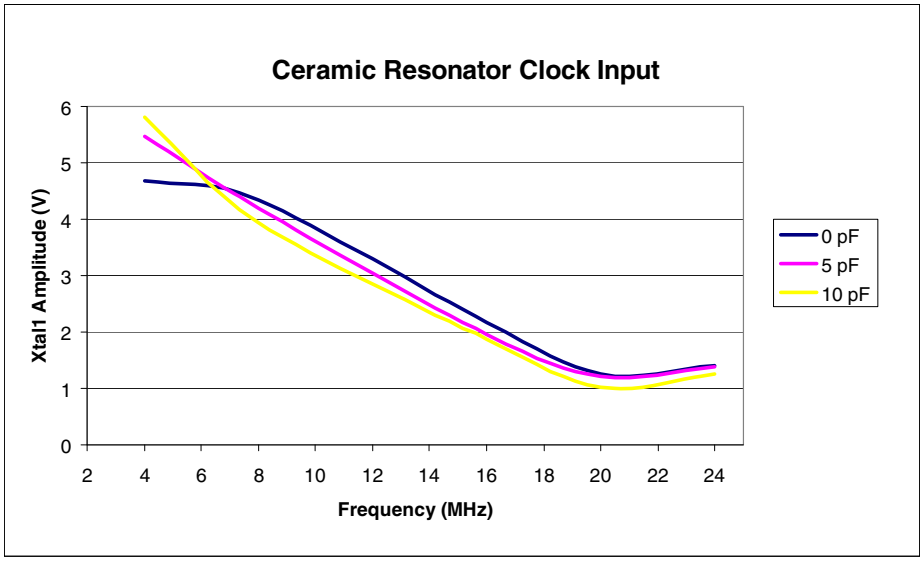
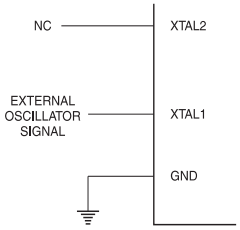


Figure 16-3. Ceramic Resonator Clock Source



To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 16-4.

Figure 16-4. External Clock Drive Configuration



17. Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. This mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Table 17-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

18. Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, external interrupt pin P3.2 or P3.3 must be kept low for at least the specified required crystal oscillator start up time. Afterwards, the interrupt service routine starts at the **rising edge** of the external interrupt pin if the SFR bit AUXR.1 is set. If AUXR.1 is reset (cleared), execution starts after a self-timed interval of 2 ms (nominal) from the **falling edge** of the external interrupt pin.

The user should not attempt to enter (or re-enter) the power-down mode for a minimum of 4 µs until after one of the following conditions has occurred: Start of code execution (after any type of reset), or Exit from power-down mode.

19. Program Memory Lock Bits

The AT89S8253 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 19-1.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operation in either the parallel or serial modes.

Table 19-1. Lock Bit Protection Modes[1]

Program Lock Bits				
	LB1	**LB2**	**LB3**	**Protection Type**
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Note: 1. U = Unprogrammed
P = Programmed

20. Programming the Flash and EEPROM

Atmel's AT89S8253 Flash microcontroller offers 12K bytes of In-System reprogrammable Flash code memory and 2K bytes of EEPROM data memory.

The AT89S8253 is normally shipped with the on-chip Flash code and EEPROM data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a parallel programming mode and a serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8253 inside the user's system. The parallel programming mode is compatible with conventional third-party Flash or EPROM programmers.

The code and data memory arrays are mapped via separate address spaces in the parallel and serial programming modes: 0000H to 2FFFH for code memory and 000H to 7FFH for data memory.

The code and data memory arrays in the AT89S8253 are programmed byte-by-byte or by page in either programming mode. To reprogram any non-blank byte in the parallel or serial mode, the user needs to invoke the Chip Erase operation first to erase both arrays since there is no built-in auto-erase capability.

Parallel Programming Algorithm: To program and verify the AT89S8253 in the parallel programming mode, the following sequence is recommended (see Figure 26-1):

1. Power-up sequence:
   a. Apply power between V_{CC} and GND pins.
   b. Set RST pin to "H".
   c. Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 ms.
2. Set $\overline{\text{PSEN}}$ pin to "L"
   a. ALE pin to "H"
   b. $\overline{\text{EA}}$ pin to "H" and all other pins to "H".
3. Raise $\overline{\text{EA}}$/VPP to 12V to enable Flash programming, erase or verification. Enable the P3.0 pull-up (10 KΩ typical) for RDY/$\overline{\text{BSY}}$ operation.
4. Apply the appropriate combination of "H" or "L" logic levels to pins P3.3, P3.4, P3.5, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
5. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   a. Apply data to pins P0.0 to P0.7 for write code operation.
6. Pulse ALE/$\overline{\text{PROG}}$ once to load a byte in the code memory array, the data memory array, or the lock bits.
7. Repeat steps 5 and 6, changing the address and data for up to 64 bytes in the code memory page or 32 bytes in the data memory (EEPROM) page. When loading a page with individual bytes, the interval between consecutive byte loads should be no longer than 150 µs. Otherwise the device internally times out and assumes that the page load sequence is completed, rejecting any further loads before the page programming sequence has finished. This timing restriction also applies to Page Write of the 64-byte User Row.
8. After the last byte of the current page has been loaded, wait for 5 ms or monitor the RDY/$\overline{\text{BUSY}}$ pin until it transitions high. The page write cycle is self-timed and typically takes less than 5 ms.
9. To verify the last byte of the page just programmed, bring pin P3.4 to "L" and read the programmed data at pins P0.0 to P0.7.

10. Repeat steps 4 through 7 changing the address and data for the entire array or until the end of the object file is reached.
11. Power-off sequence:
    a. Tri-state the address and data inputs.
    b. Disable the P3.0 pullup used for RDY/$\overline{\text{BUSY}}$ operation.
    c. Set XTAL1 to “L”.
    d. Set RST and $\overline{\text{EA}}$ pins to “L”.
    e. Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The AT89S8253 features $\overline{\text{DATA}}$ Polling to indicate the end of any programming cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last loaded byte will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{DATA}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. Pin P3.0 is pulled Low after ALE goes High during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled High again when programming is done to indicate READY. P3.0 needs an external pullup (typical 10 KΩ) when functioning as RDY/$\overline{\text{BSY}}$.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel and serial programming modes.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, Chip Erase is initiated by using the proper combination of control signals. The code and data arrays are written with all “1”s during the Chip Erase operation. The User Row will also be erased if the UsrRowProEn fuse (Fuse3) = 0 (enabled state).

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, Chip Erase is self-timed and also takes about 8 ms.

During Chip Erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can be disabled via both the Parallel/Serial Programming Modes, but can only be enabled via the Parallel mode.

The AT89S8253 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 73H indicates AT89S8253

21. Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

22. Serial Downloading

Both the code and data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction must be executed first before other operations can be executed.

The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The code and data memory arrays have separate address spaces:

0000H to 2FFFH for code memory and 000H to 7FFH for data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 1.5 MHz.

23. Serial Programming Algorithm

To program and verify the AT89S8253 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to “H”.

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 12 MHz clock to XTAL1 pin and wait for at least 10 ms with RST pin high and P1.7 (SCK) low.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The code or data array is programmed one byte or one page at a time by supplying the address and data together with the appropriate Write instruction. The write cycle is self-timed and typically takes less than 4.0 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

1. Set XTAL1 to “L” (if a crystal is not used).
2. Set RST to “L”.
3. Turn V_{CC} power off.

24. Serial Programming Instruction

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 24-1.

Table 24-1. Serial Programming Instruction Set

Instruction	Instruction Format					Operation
	Byte 1	Byte 2	Byte 3	Byte 4	Byte n	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx		Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx		Chip Erase both the 12K and 2K memory arrays
Write **Program** Memory (**Byte** Mode)	0100 0000	xx A13 A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0		Write data to Program Memory – Byte Mode
Read **Program** Memory (**Byte** Mode)	0010 0000	xx A13 A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0		Read data from Program Memory – Byte Mode
Write **Program** Memory (**Page** Mode)	0101 0000	xx A13 A12 A11 A10 A9 A8	A7 A6 00 0000	Byte 0 ... Byte 63		Write data to Program Memory – Page Mode (64 bytes)
Read **Program** Memory (**Page** Mode)	0011 0000	xx A13 A12 A11 A10 A9 A8	A7 A6 00 0000	Byte 0 ... Byte 63		Read data from Program Memory – Page Mode (64 bytes)
Write **Data** Memory (**Byte** Mode)	1100 0000	xxxx x A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0		Write data to Data Memory – Byte Mode
Read **Data** Memory (**Byte** Mode)	1010 0000	xxxx x A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0		Read data from Data Memory – Byte Mode
Write **Data** Memory (**Page** Mode)	1101 0000	xxxx x A10 A9 A8	A7 A6 A5 0 0000	Byte 0 ... Byte 31		Write data to Data Memory – Page Mode (32 bytes)
Read **Data** Memory (**Page** Mode)	1011 0000	xxxx x A10 A9 A8	A7 A6 A5 0 0000	Byte 0 ... Byte 31		Read data from Data Memory – Page Mode (32 bytes)
Write User Fuses	1010 1100	0001 FUSE4 FUSE3 FUSE2 FUSE1	xxxx xxxx	xxxx xxxx		Write user fuse bits (refer to next page for the fuse definitions)
Read User Fuses	0010 0001	xxxx xxxx	xxxx xxxx	xxxx FUSE4 FUSE3 FUSE2 FUSE1		Read back status of user fuse bits
Write Lock Bits	1010 1100	1110 0 LB3 LB2 LB1	xxxx xxxx	xxxx xxxx		Write the lock bits (write a “0” to lock)
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxxx x LB3 LB2 LB1		Read back current status of the lock bits (a programmed lock bit reads back as a “0”)
Write User Sgn. Byte	0100 0010	xxxx xxxx	xx A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0		
Read User Sgn. Byte	0010 0010	xxxx xxxx	xx A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0		
Write User Sgn. Page	0101 0010	xxxx xxxx	xxxx xxxx	Byte 0 ... Byte 63		
Read User Sgn. Page	0011 0010	xxxx xxxx	xxxx xxxx	Byte 0 ... Byte 63		
Read ATMEL Sgn. Byte	0010 1000	xxxx xxxx	xx A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0		Read Signature Byte

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at pin XTAL1.

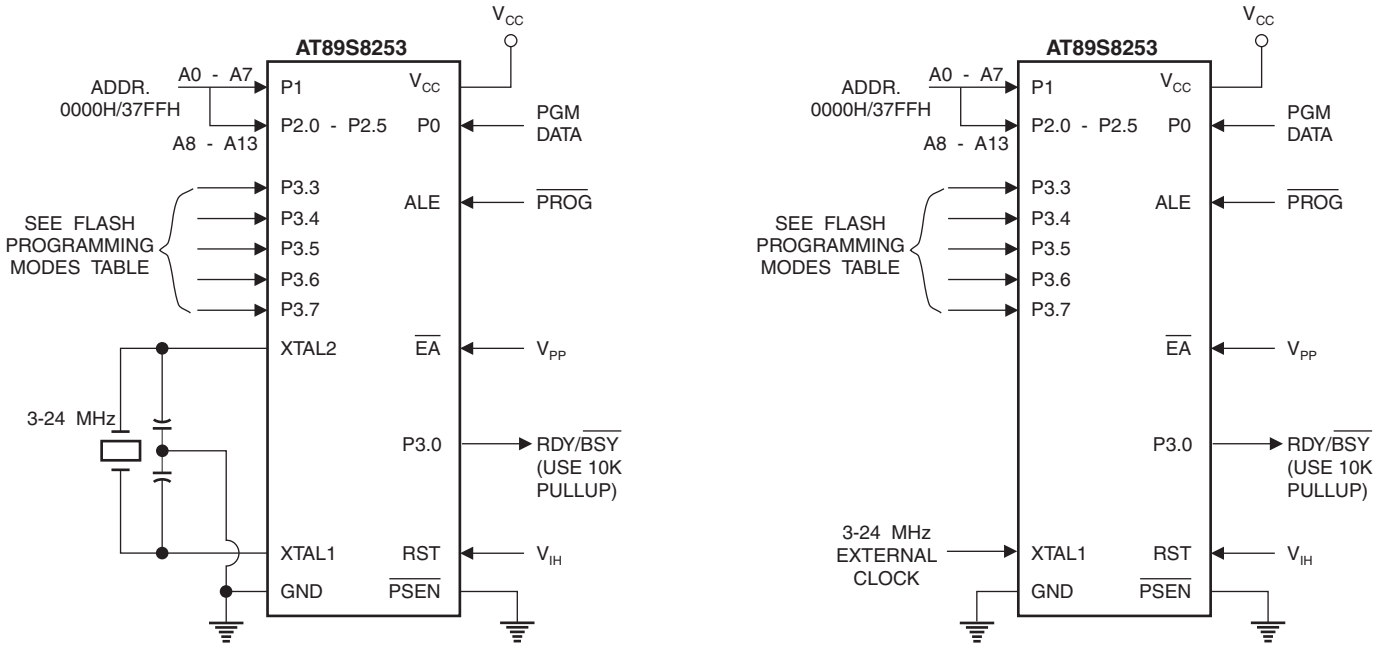
For Page Read/Write, the data always starts from byte 0 to 31 or 63. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 32 or 64 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

25. Flash and EEPROM Parallel Programming Modes

Mode		RST	PSEN	ALE	EA	P3.3	P3.4	P3.5	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0, P1.7:0
Serial Prog. Modes[1]		H	h	h								
Chip Erase[2]		H	L	1.0 µs	12V	H	L	H	L	L	X	X
Page Write[3][4][5]	12K **Code**	H	L	1.0 µs	12V	L	H	H	H	H	DI	ADDR
Read	12K **Code**	H	L	H	12V	L	L	H	H	H	DO	ADDR
Page Write[3][4][6]	2K **Data**	H	L	1.0 µs	12V	L	H	L	H	H	DI	ADDR
Read	2K **Data**	H	L	H	12V	L	L	L	H	H	DO	ADDR
Write Lock Bits[2][4]	Bit - 1	H	L	1.0 µs	12V	H	L	H	H	L	D0 = 0	X
	Bit - 2										D1 = 0	X
	Bit - 3										D2 = 0	X
Read Lock Bits	Bit - 1	H	L	H	12V	H	H	H	L	L	D0	X
	Bit - 2										D1	X
	Bit - 3										D2	X
Page Write[3][4][5]	User Row	H	L	1.0 µs	12V	H	L	H	H	H	DI	0 - 3FH
Read	User Row	H	L	H	12V	L	L	H	L	H	DO	0 - 3FH
Read	Sig. Row	H	L	H	12V	L	L	H	L	L	DO	0 - 3FH
Write Fuse[2][4][7]	Fuse1: SerialPrgEn	H	L	1.0 µs	12V	L	H	H	L	H	D0 = 0	X
	Fuse1: SerialPrgDis										D0 = 1	X
	Fuse2: x2 ClockEn										D1 = 0	X
	Fuse2: x2 ClockDis										D1 = 1	X
	Fuse3: UsrRowPrgEn										D2 = 0	X
	Fuse3: UsrRowPrgDis										D2 = 1	X
	Fuse4: External Clock En										D3 = 0	X
	Fuse4: Crystal Clock En										D3 = 1	X
Read Fuse	SerialPrg (Fuse1)	H	L	H	12V	H	H	H	L	H	D0	X
	x2 Clock (Fuse2)										D1	X
	UsrRow Prg (Fuse3)										D2	X
	Clock Select (Fuse4)										D2	X

Notes:
1. See detailed timing for Serial Programming Mode.
2. Internally timed for 8.0 ms.
3. Internally timed for 8.0 ms. Programming begins 150 µs (minimum) after the last write pulse.
4. P3.0 is pulled low during programming to indicate RDY/$\overline{BSY}$
5. 1 to 64 bytes can be programmed at a time per page.
6. 1 to 32 bytes can be programmed at a time per page.
7. Fuse Definitions:
   Fuse1 (Serial Programming Fuse): This fuse enables/disables the serial programming mode (ISP).
   Fuse2 (x2 Mode Selection Fuse): This fuse enables/disables the internal x2 clock mode.
   Fuse3 (User Row Access Fuse): This fuse enables/disables writing to the programmable user row.
   Fuse4 (Clock Selection Fuse): This fuse selects between an external clock source and a quartz crystal as the clock input.

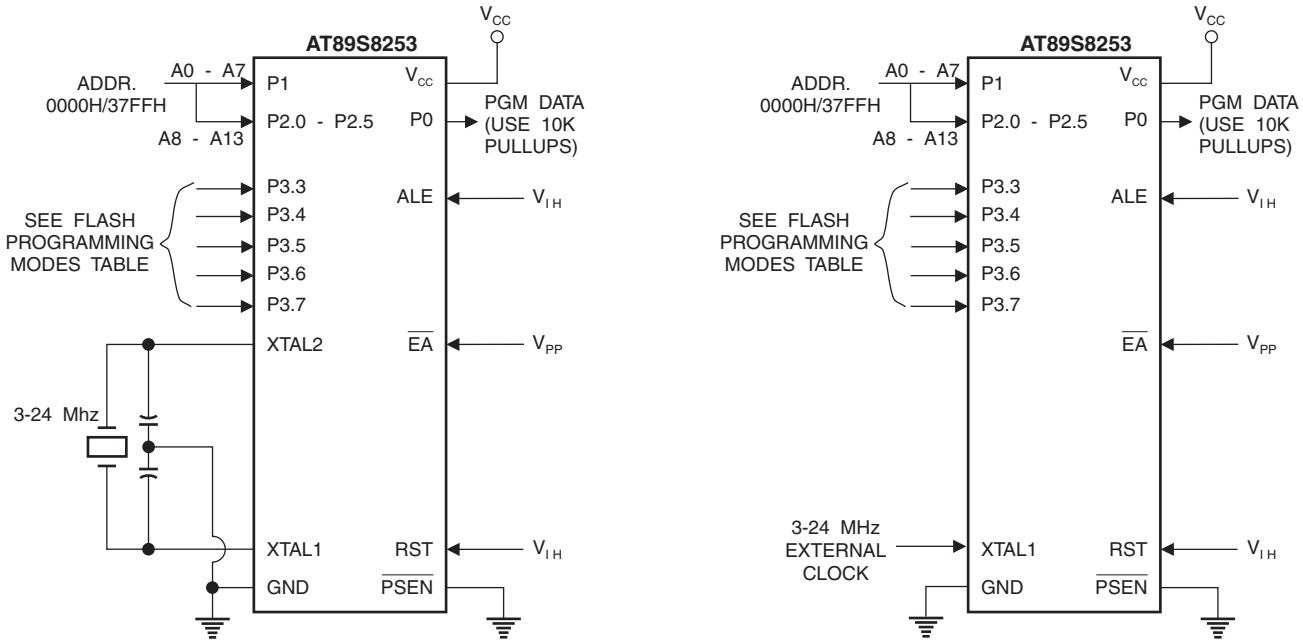
Figure 25-1. Programming the Flash/EEPROM Memory **(Parallel Mode)**



Oscillator Bypass Fuse (Fuse4) Off

Oscillator Bypass Fuse (Fuse4) On

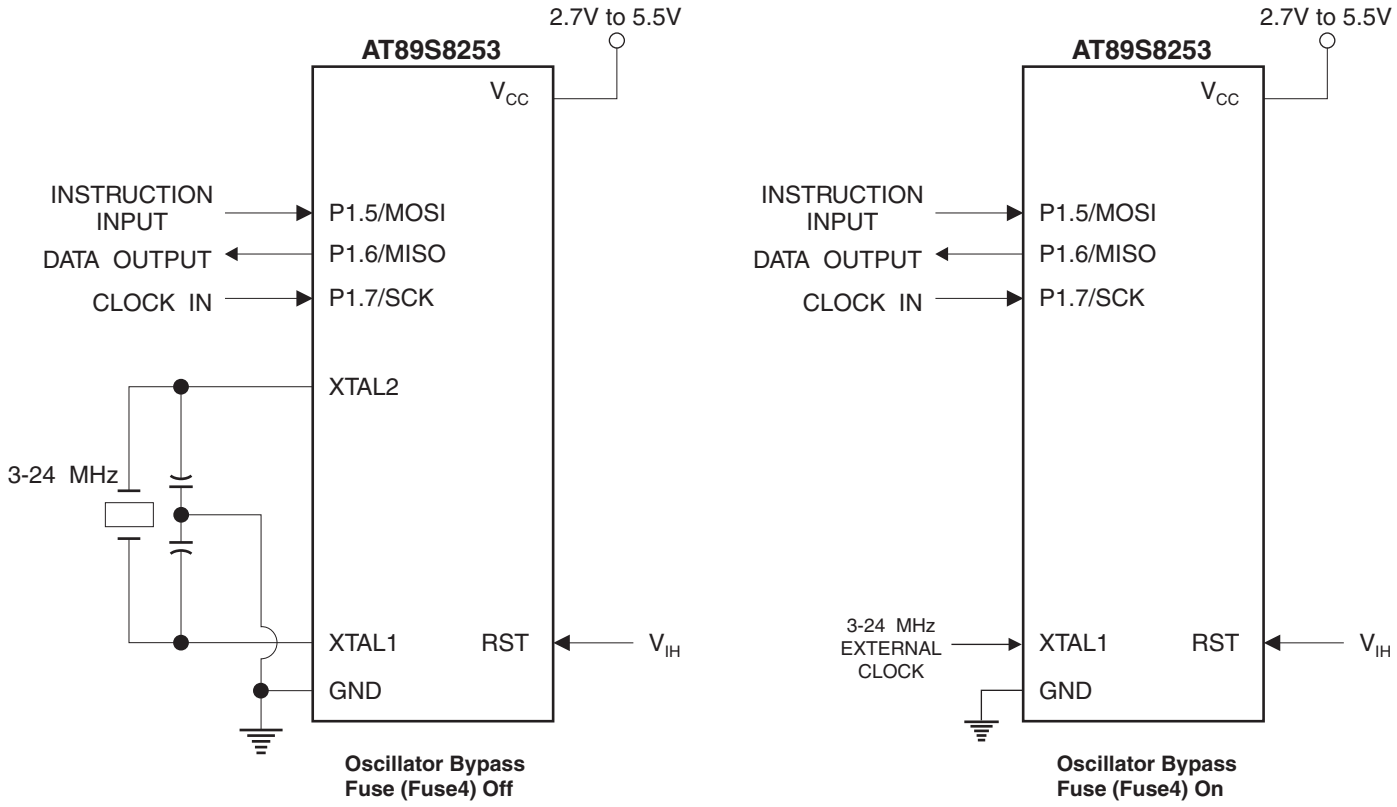
Figure 25-2. Verifying the Flash/EEPROM Memory **(Parallel Mode)**



Oscillator Bypass Fuse (Fuse4) Off

Oscillator Bypass Fuse (Fuse4) On

Figure 25-3. Flash/EEPROM **Serial Downloading**



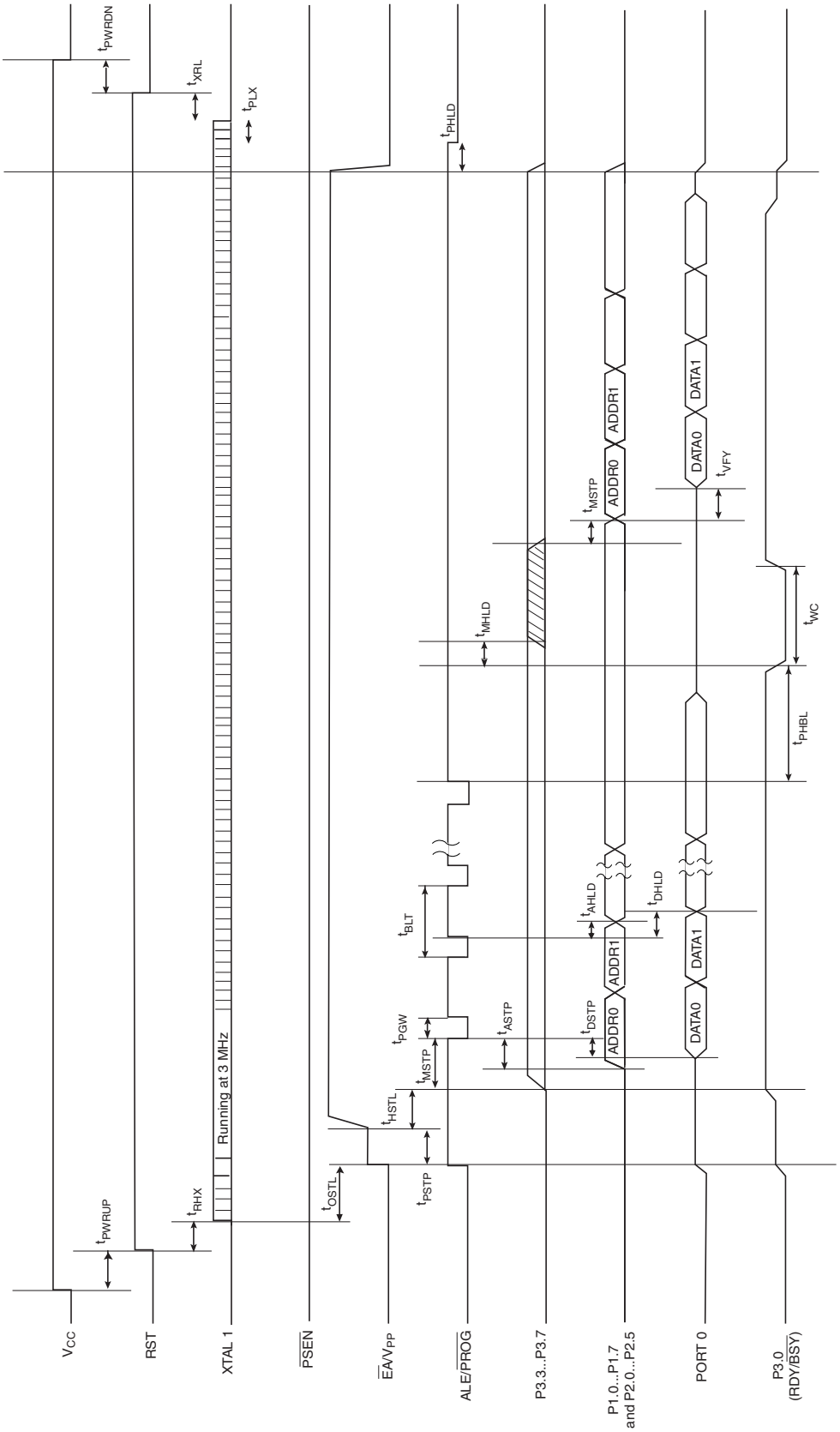
26. Flash Programming and Verification Characteristics – Parallel Mode

T_A = 20°C to 30°C, V_{CC} = 4.0V to 5.5V

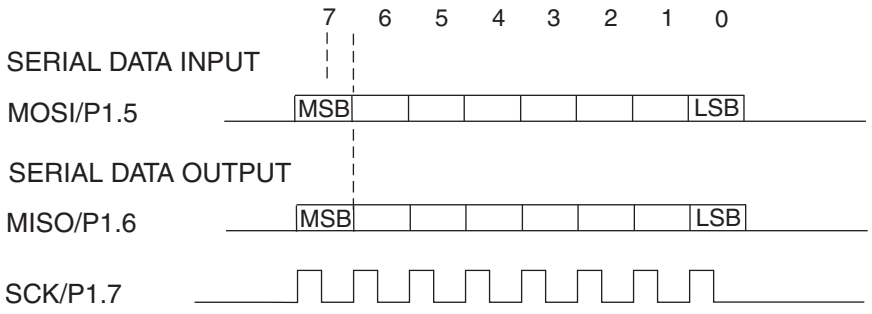
Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{PWRUP}	Power On to RST High (1)	10		µs
t_{RHX}	RST High to XTAL Start	10		µs
t_{OSTL}	Oscillator Settling Time	10		ms
t_{HSTL}	High Voltage Settling Time	10		µs
t_{MSTP}	Mode Setup to $\overline{PROG}$ Low	1		µs
t_{ASTP}	Address Setup to $\overline{PROG}$ Low	1		µs
t_{DSTP}	Data Setup to $\overline{PROG}$ Low	1		µs
t_{PGW}	$\overline{PROG}$ Width	1		µs
t_{AHLD}	Address Hold after $\overline{PROG}$	1		µs
t_{DHLD}	Data Hold after $\overline{PROG}$	1		µs
t_{BLT}	Byte Load Period	1	150	µs
t_{PHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		256	µs
t_{WC}	Write Cycle Time(2)		4.5	ms
t_{MHLD}	Mode Hold After $\overline{BUSY}$ Low	10		µs
t_{VFY}	Address to Data Verify Valid		1	µs
t_{PSTP}	$\overline{PROG}$ Setup to V_{PP} High	10		µs
t_{PHLD}	$\overline{PROG}$ Hold after V_{PP} Low	10		µs
t_{PLX}	$\overline{PROG}$ Low to XTAL Halt	1		µs
t_{XRL}	XTAL Halt to RST Low	1		µs
t_{PWRDN}	RST Low to Power Off	1		µs

Notes: 1. Power On occurs once V_{CC} reaches 2.4V.
2. 9 ms if Chip Erase.

Figure 26-1. Flash/EEPROM Programming and Verification Waveforms – Parallel Mode



27. Serial Downloading Waveforms (SPI Mode 1 —> CPOL = 0, CPHA = 1)



28. Serial Programming Characteristics

Figure 28-1. Serial Programming Timing

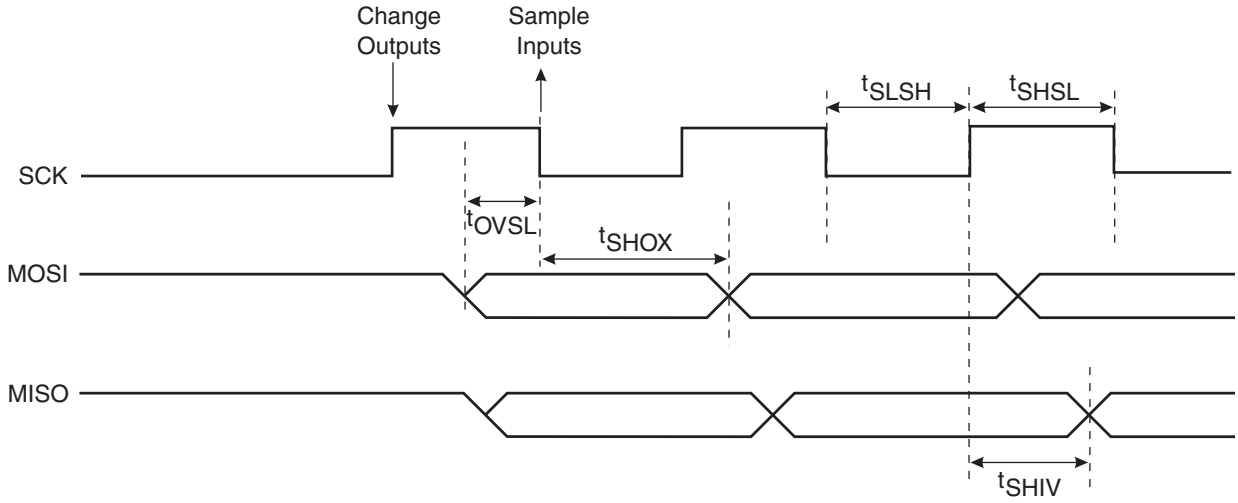


Table 28-1. Serial Programming Characteristics, T_A = -40·C to 85·C, V_{CC} = 2.7V - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		24	MHz
t_{CLCL}	Oscillator Period	41.6		33.3	ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSL}	MOSI Setup to SCK Low	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK Low	2 t_{CLCL}			ns
t_{SHIV}	SCK High to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			9	ms
t_{SWC}	Serial Page Write Cycle Time			4.5	ms

29. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

30. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 2.7 to 5.5V, unless otherwise noted

Symbol	Parameter	Condition	Min	Max
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5V	0.2 V_{CC} - 0.1V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5V	0.2 V_{CC} - 0.3V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9V	V_{CC} + 0.5V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5V
V_{OL}	Output Low-voltage[1]	I_{OL} = 10 mA, V_{CC} = 4.0V, T_A = 85°C		0.5V
V_{OH}	Output High-voltage When Weak Pull Ups are Enabled (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, T_A = 85°C	2.4V	
		I_{OH} = -25 µA, T_A = 85°C	0.75 V_{CC}	
		I_{OH} = -10 µA, T_A = 85°C	0.9 V_{CC}	
V_{OH1}	Output High-voltage When Strong Pull Ups are Enabled (Port 0 in External Bus Mode, P1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = -40 mA, T_A = 85°C	2.4V	
		I_{OH} = -25 mA, T_A = 85°C	0.75 V_{CC}	
		I_{OH} = -10 mA, T_A = 85°C	0.9 V_{CC}	
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.45V, V_{CC} = 5.5V, T_A = -40°C		-50 µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V_{IN} = 2V, V_{CC} = 5.5V, T_A = -40°C		-352 µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45V< V_{IN} < V_{CC}		±10 µA
RRST	Reset Pull-down Resistor		50 KΩ	150 KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10 pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5.5V, T_A = -40°C		10 mA
		Idle Mode, 12 MHz, V_{CC} = 5.5V, T_A = -40°C		3.5 mA
	Power-down Mode[2]	V_{CC} = 5.5V, T_A = -40°C		100 µA
		V_{CC} = 4.0V, T_A = -40°C		20 µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA,
   Maximum I_{OL} per 8-bit port:15 mA,
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

31. AC Characteristics

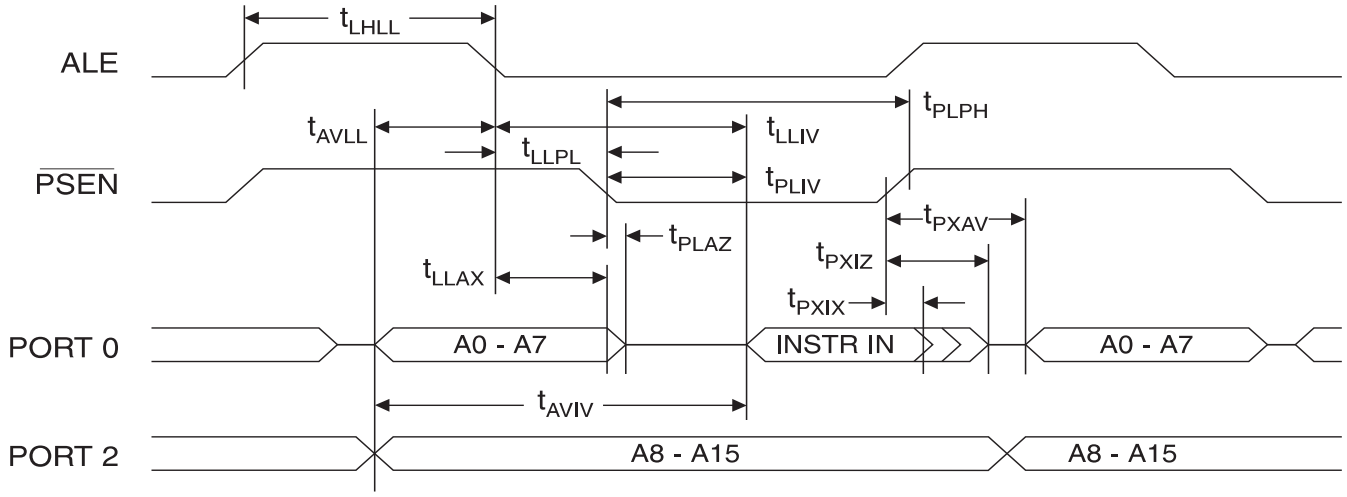
The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 2.7 to 5.5V, unless otherwise noted.

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

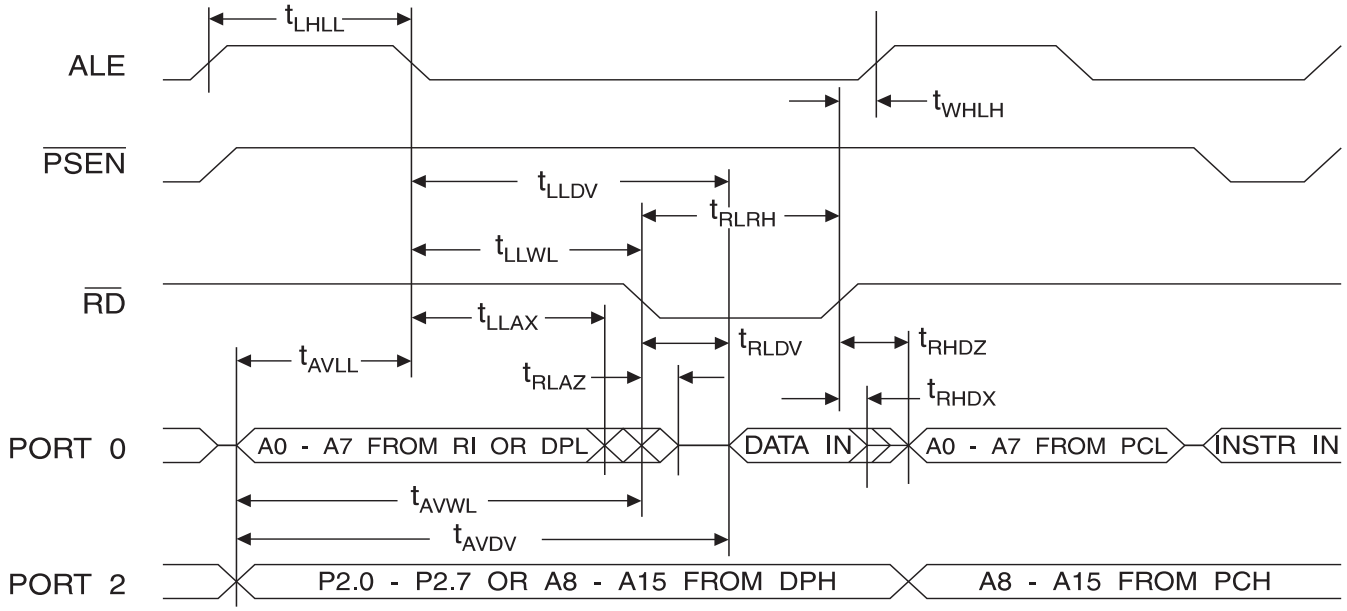
31.1 External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 12		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 12		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 16		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 50	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 12		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 12		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 50	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	-10		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		t_{CLCL} - 20	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 4		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 50	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		20	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 50	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 20	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 50	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 50	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 24	$3t_{CLCL}$	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 12		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	$2t_{CLCL}$ - 24		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$8t_{CLCL}$ - 24		ns
t_{WHQX}	Data Hold after $\overline{WR}$	$2t_{CLCL}$ - 24		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 10	t_{CLCL} + 20	ns

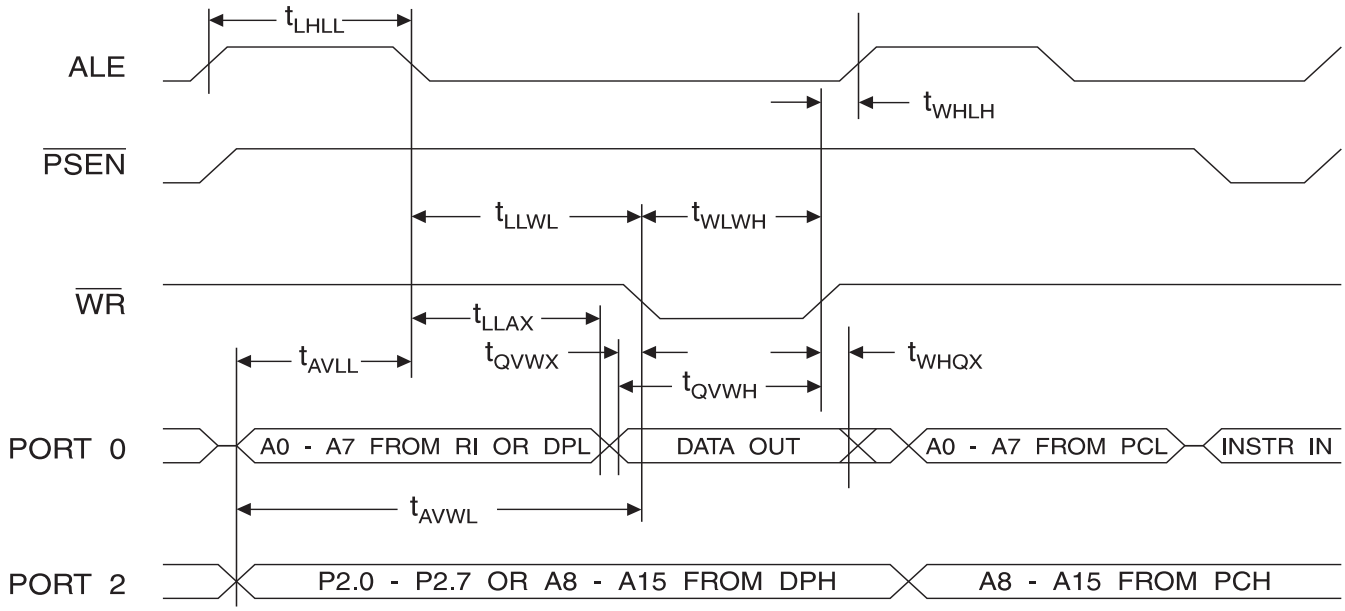
32. External Program Memory Read Cycle



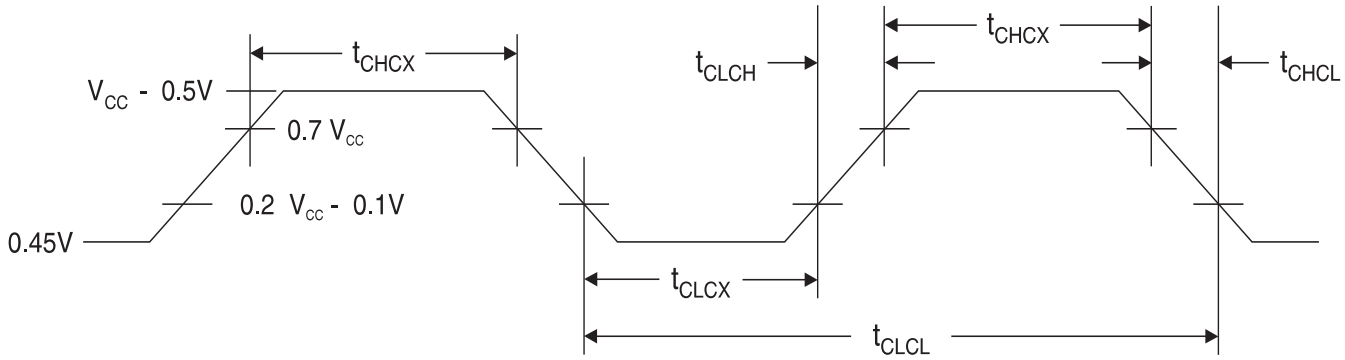
33. External Data Memory Read Cycle



34. External Data Memory Write Cycle



35. External Clock Drive Waveforms



36. External Clock Drive

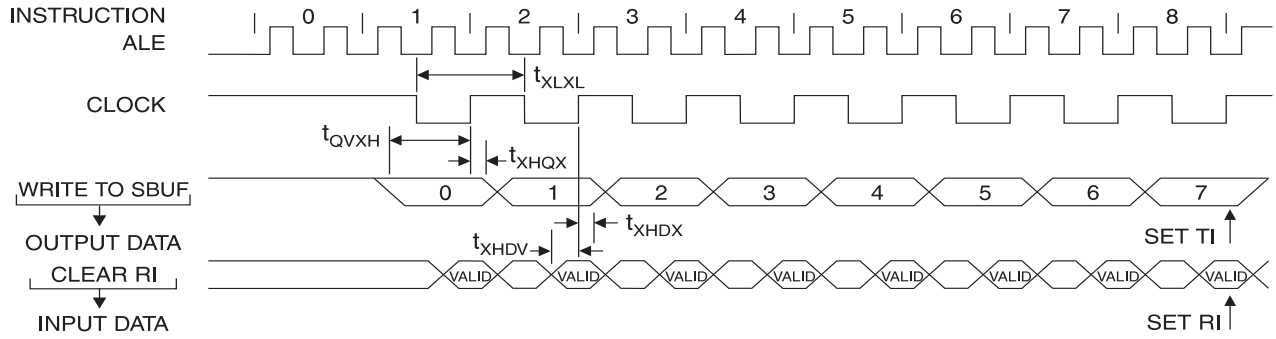
Symbol	Parameter	V_{CC} = 2.7V to 5.5V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

37. Serial Port Timing: Shift Register Mode Test Conditions

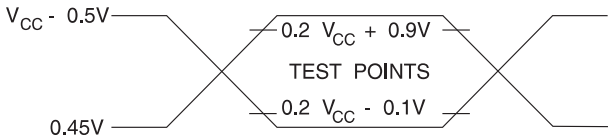
The values in this table are valid for V_{CC} = 2.7V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$ -15		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ -15		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ -15		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	t_{CLCL}		ns
t_{XHDV}	Input Data Valid to Clock Rising Edge	0		ns

38. Shift Register Mode Timing Waveforms



39. AC Testing Input/Output Waveforms[1]

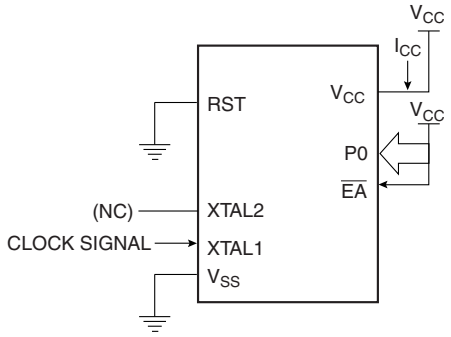


Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

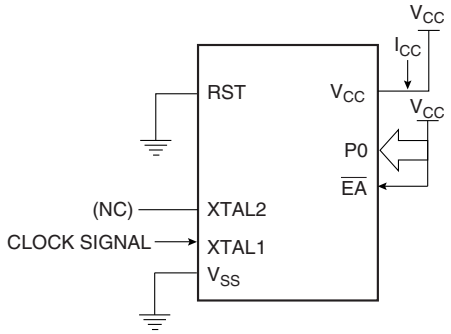
40. Float Waveforms[1]

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

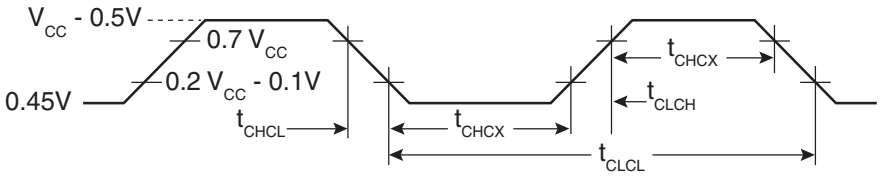
41. I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected



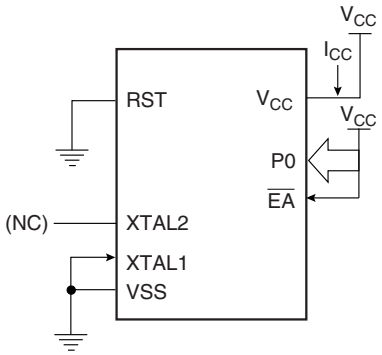
42. I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



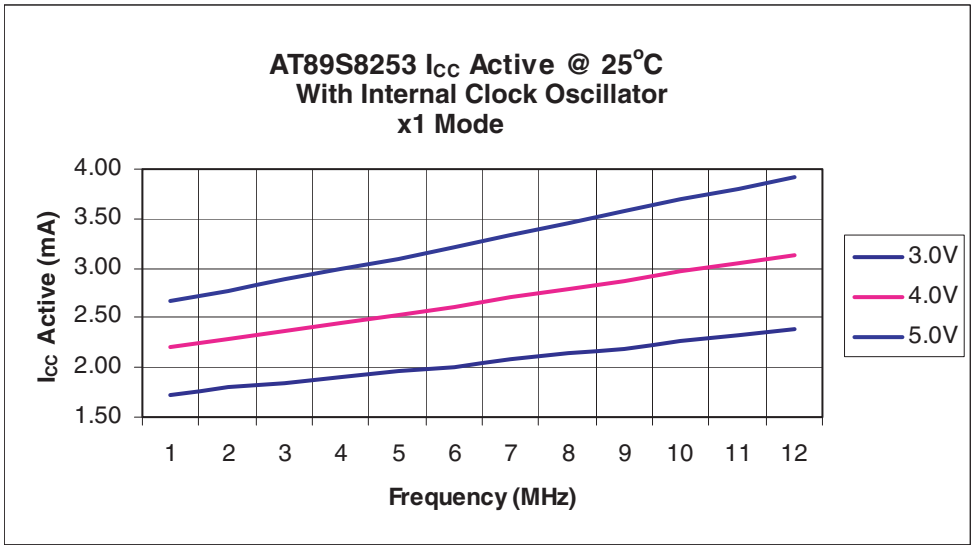
43. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns

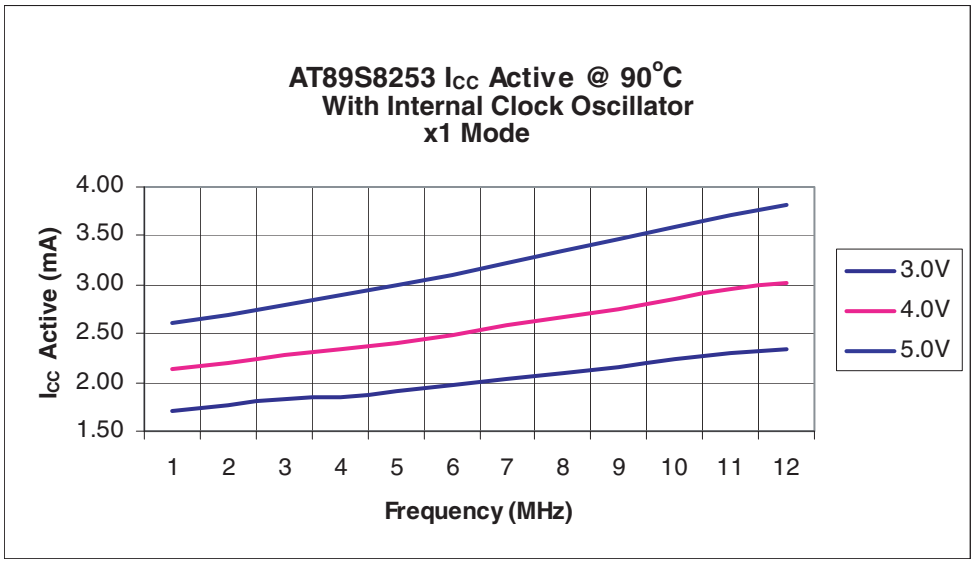


44. I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{CC} = 2V to 5.5V

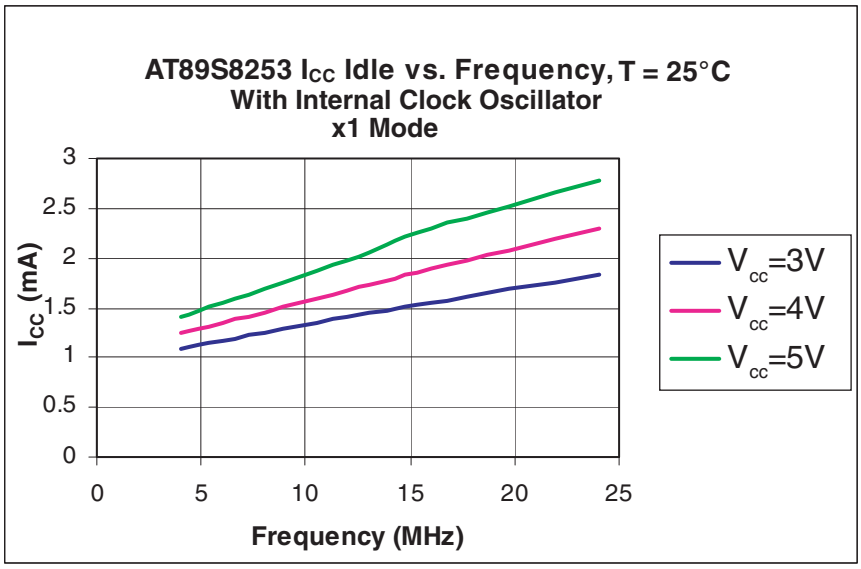


45. I_{CC} (Active Mode) Measurements

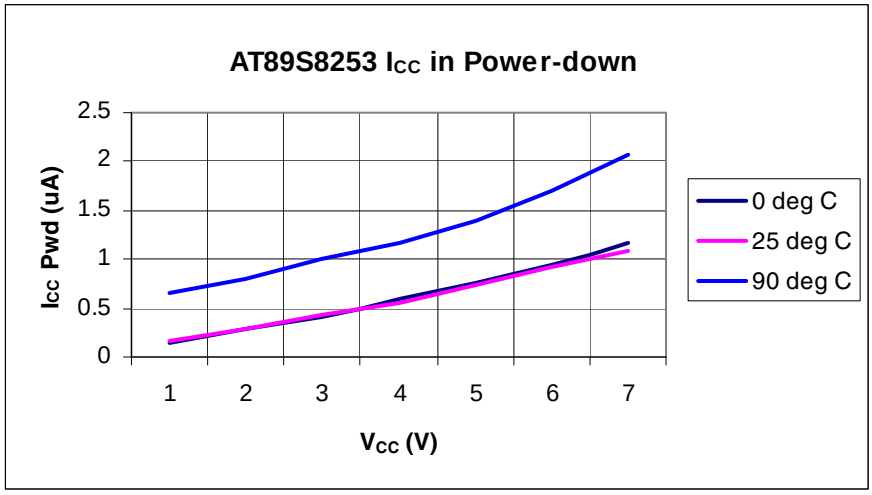




46. I_{CC} (Idle Mode) Measurements



47. I_{CC} (Power Down Mode) Measurements



48. Ordering Information

48.1 Standard Package

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	2.7V to 5.5V	AT89S8253-24AC AT89S8253-24JC AT89S8253-24PC AT89S8253-24PSC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)
	2.7V to 5.5V	AT89S8253-24AI AT89S8253-24JI AT89S8253-24PI AT89S8253-24PSI	44A 44J 40P6 42PS6	Industrial (-40°C to 85°C)

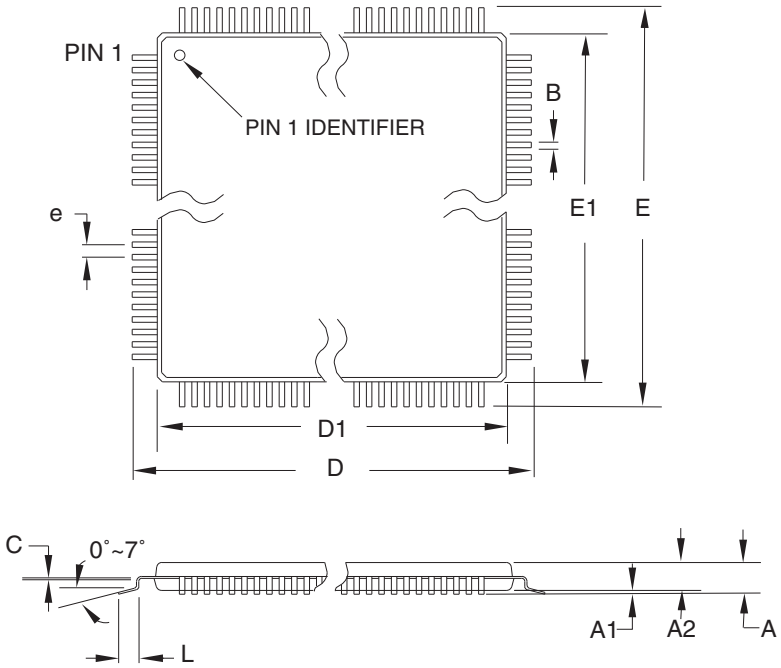
48.2 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	2.7V to 5.5V	AT89S8253-24AU AT89S8253-24JU AT89S8253-24PU AT89S8253-24PSU	44A 44J 40P6 42PS6	Industrial (-40°C to 85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flat Package (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

49. Package Information

49.1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

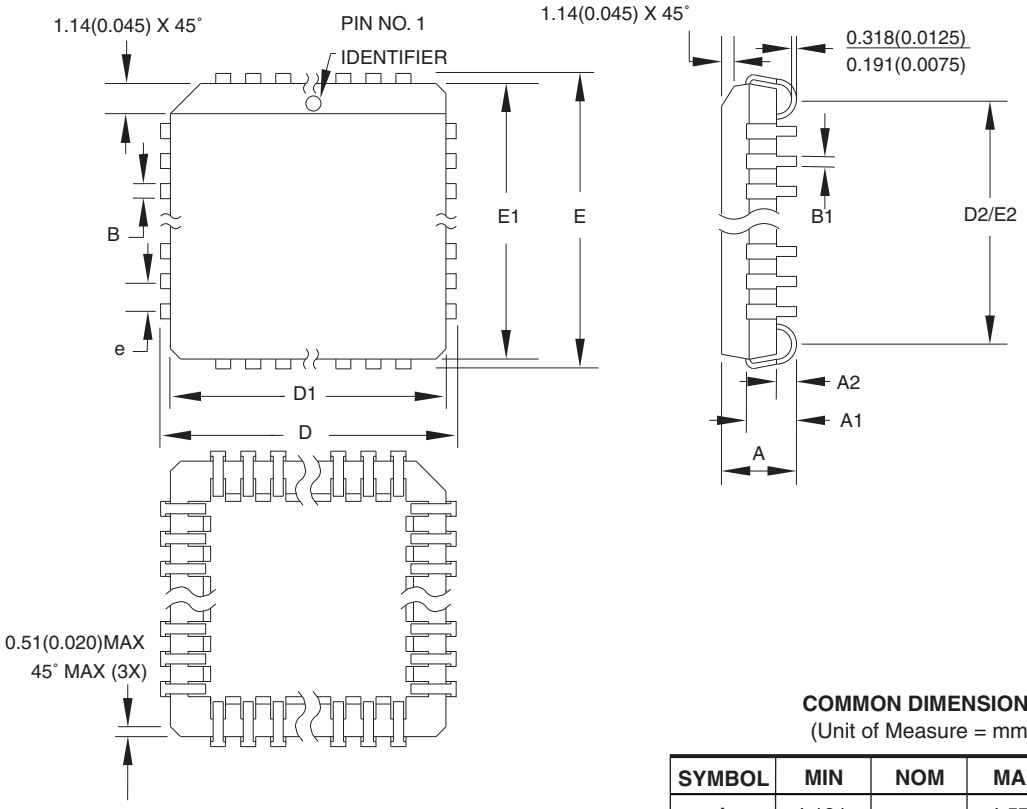
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

49.2 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

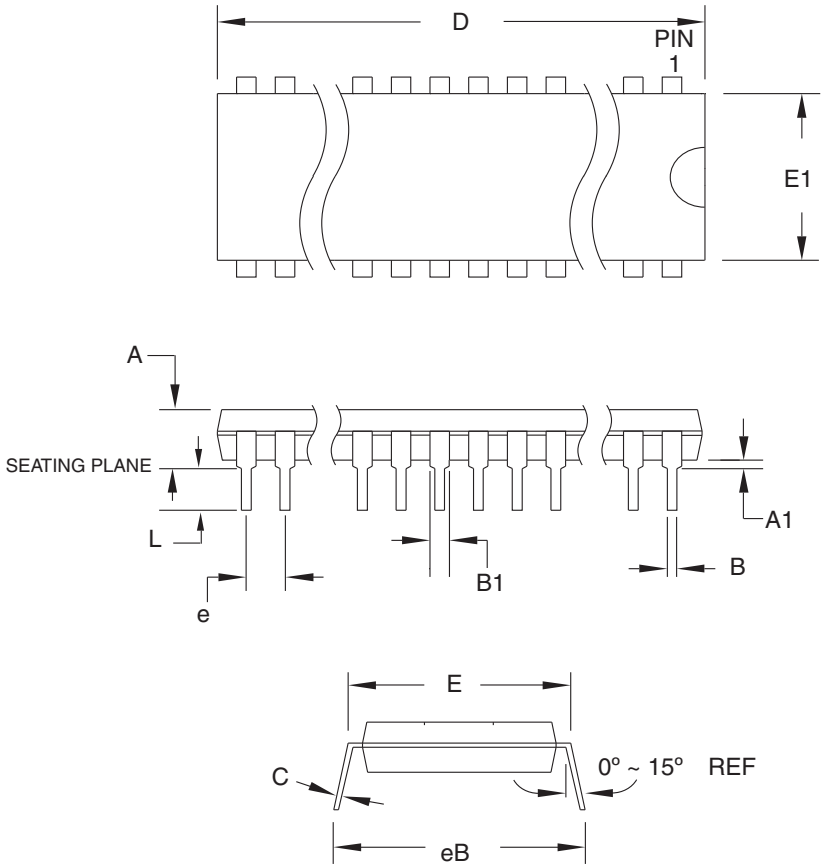
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

49.3 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

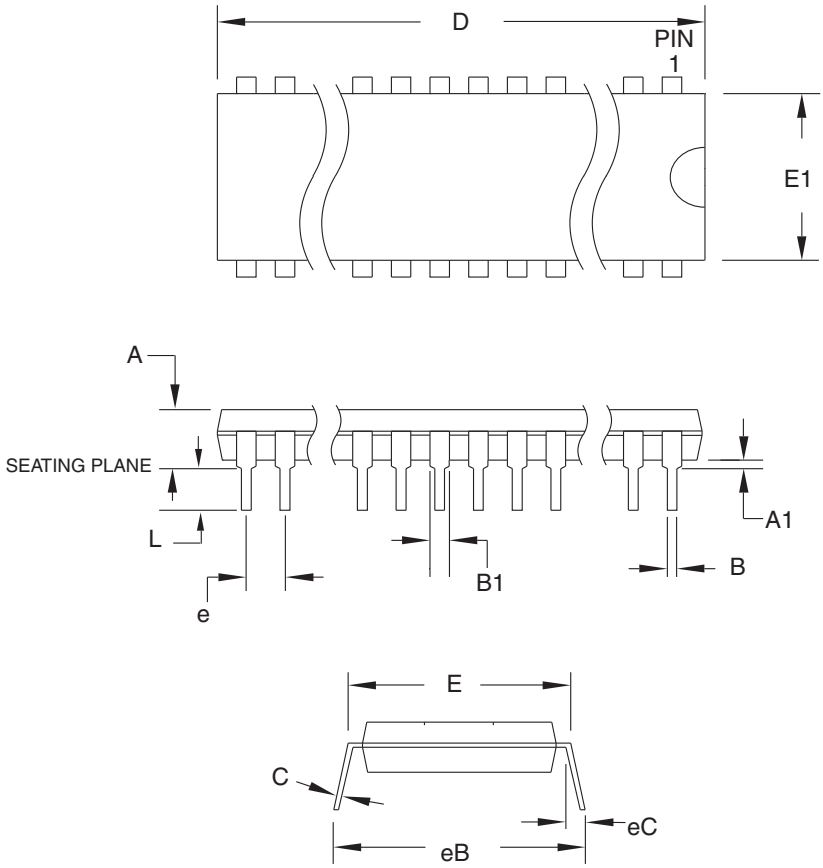
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

49.4 42PS6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = Inch)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.200	
A1	0.020	–	–	
D	1.440	1.450	1.460	Note 2
E	0.600	–	0.630	
E1	0.500	0.540	0.570	Note 2
B	0.015	0.018	0.022	
B1	0.035	0.040	0.045	
L	0.100	0.130	0.140	
C	0.009	0.010	0.015	
eB	–	–	0.730	
eC	0.000	–	0.060	
e	0.70 TYP			

Notes: 1. This package conforms to JEDEC reference MS-020, Variation AB.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/3/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (Shrink 0.070"/0.600" Row Space) Plastic Dual Inline Package (PDIP)	42PS6	B

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